

# **W83791SD**

## **Winbond H/W**

### **Monitoring IC**



## W83791SD Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1	n.a.			n.a.	All version before 0.50 are for internal use.
2	n.a.	01/Jan	0.5	n.a.	First publication.
3	n.a.	02/Apr	1.0	1.0	Change all version include version on web site to 1.0
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## 1. GENERAL DESCRIPTION

W83791SD is a programmable speech synthesizer with 9-bit current DAC output that can connect to speaker or LINE\_OUT by the AC'97 audio codec. It supports 1 CPU present or absent event trap, 5 external event traps, and 127 internal programmable event traps to trigger maximum 133 different speech output. If more than two events happen simultaneously, the priority set is: SLOTOCC# > EVNTRP1 > EVNTRP2 > EVNTRP3 > EVNTRP4 > EVNTRP5 > 127 Programmable events (Bank0 index 09h).

For the application of error messages from BIOS, 127 Programmable events are enabled with a watch dog timer. The time interval is programmable and events will be triggered when time out.

External flash memory interface with Winbond W55FXX is flexible to change warning voice message and support on-line programming flash data through I<sup>2</sup>C<sup>TM</sup> interface. An external resistor is added to provide ring oscillator.

Through the application software or BIOS, the users can edit and change the voice database in the serial flash chip by themselves under O.S.. A free Windows AP --- Voice Editor<sup>TM</sup> is provided for the voice editing, which can accept the \*.wav file as the voice database resource. Users can replace the voice with which they like through the S/W.

W83791SD also provides two address setting pins A0 & A1 for different I<sup>2</sup>C<sup>TM</sup> address and can be connected up to 4 devices if necessary

## 2. FEATURES

### 2.1. Speech Item

- Programmable speech synthesizer
- New high fidelity synthesis algorithm
- Build in 8-bit current D/A converter
- Instruction cycle  $\leq 400 \mu\text{S}$  typically
- Section control provided in each voice section
  - Variable frequency: 4.8/6/8/12 KHz
- External resistor for ring oscillator
- 1 CPU present or absent trigger input
- 5 External trigger inputs
- 127 Internal programmable trigger inputs with a watch dog timer
- Programmable 0-255 seconds timeout trigger inputs



## 2.2. General

- I<sup>2</sup>C™ serial bus interface
- 2 pins (A0, A1) to provide selectable address setting for application of multiple devices (up to 4 devices) wired through I<sup>2</sup>C™ interface
- Winbond hardware monitoring application software (Voice Editor™ ) support, for both Windows 95/98/ME/2000 and Windows NT 4.0/5.0
- Internal clock Oscillator with 3M Hz
- 5V VDD operation

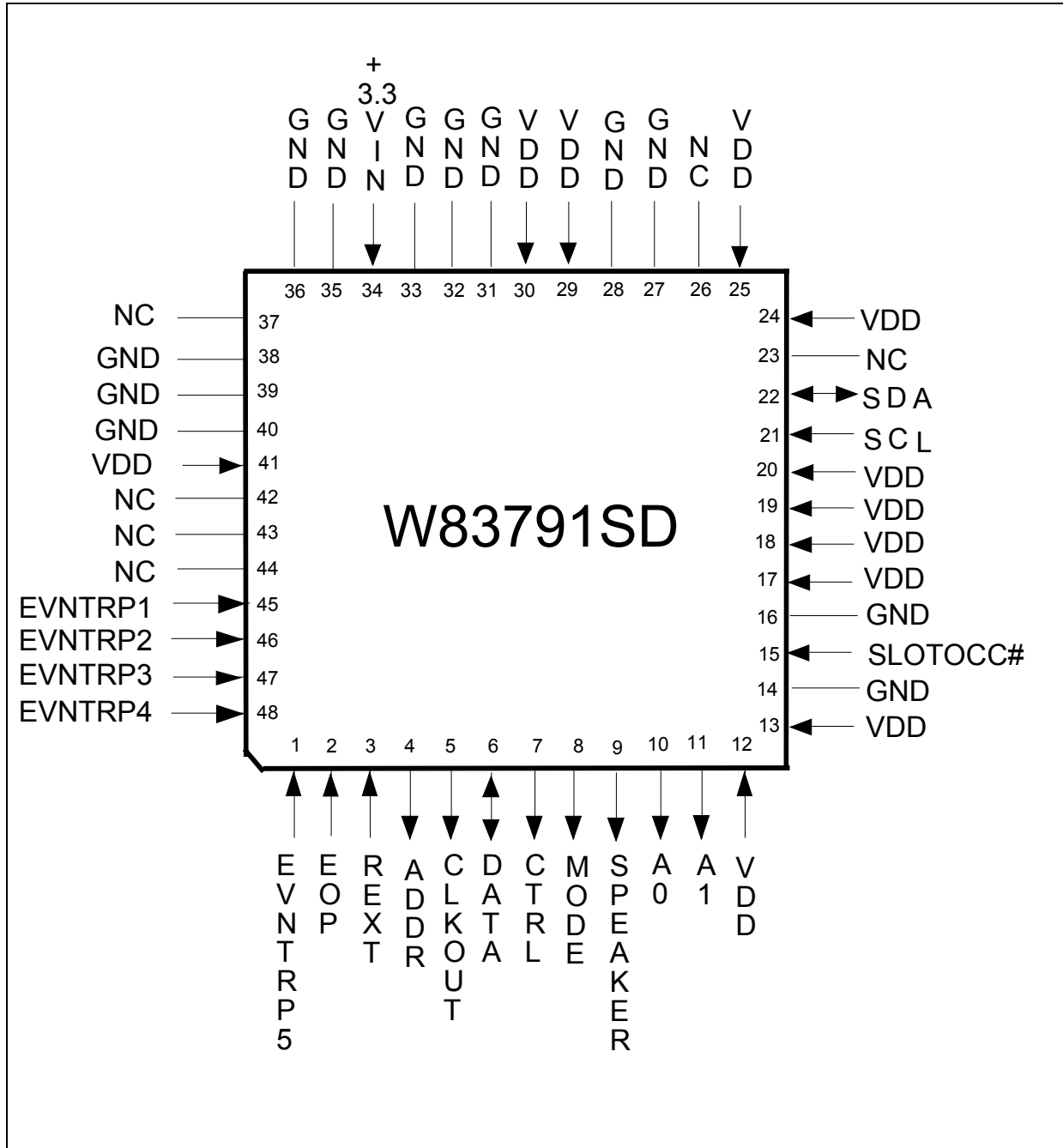
## 2.3. Package

- 48-pin LQFP

## 3. KEY SPECIFICATIONS

- Supply Voltage                      5V
- Operating Supply Current        5 mA typ.

## 4. PIN CONFIGURATION





## 5. PIN DESCRIPTION

- I/O<sub>12t</sub> - TTL level bi-directional pin with 12 mA source-sink capability
- I/O<sub>12ts</sub> - TTL level and schmitt trigger with 12 mA source-sink capability
- I/OD<sub>8ts</sub> - TTL level and schmitt trigger open drain output with 8 mA sink capability
- OUT<sub>12</sub> - Output pin with 12 mA source-sink capability
- IN<sub>t</sub> - TTL level input pin
- IN<sub>ts</sub> - TTL level input pin and schmitt trigger
- AIN - Input pin(Analog)

Pin Name	Pin No.	Type	Description
EVNTRP5	1	IN <sub>t</sub>	Event trapping to selection speech output sound.
EOP	2	IN <sub>t</sub>	End of Process signal input from cascaded Flash.
REXT	3	IN <sub>t</sub>	Resistor(Rosc) connect to VSB used to adjust ring oscillator frequency.
ADDR	4	OUT <sub>12</sub>	Speech address pulse output, connect to W55FXX. When this pin translates from logic high to logic low, it will latch the data pin 6 and shift it into a speech flash address counter.
CLKOUT	5	OUT <sub>12</sub>	Speech clock output, for speech data read-out and write-in, connect to W55FXX. When this pin translates from logic high to logic low, the data pin 6 will be latched by this clock.
DATA	6	I/O <sub>12t</sub>	Serial data input/output, connect to W55FXX. The pin is latched by CLKOUT and ADDR acted as speech data and address respectively.
CTRL	7	OUT <sub>12</sub>	Output clock numbers of this pin decide which mode is selected. Connect to W55FXX.
MODE	8	OUT <sub>12</sub>	Output mode signal to W55FXX serial Flash.
SPEAKER	9	OUT <sub>12</sub>	Current type output driving an external speaker. The function is only working in VSB 5V OK.
A0	10	IN <sub>ts</sub>	I <sup>2</sup> C device address bit0 trapping during 5VDD power on.
A1	11	IN <sub>ts</sub>	I <sup>2</sup> C device address bit1 trapping during 5VDD power on.
VDD (5V)	12,13,17, 18,19,20, 24,25,29, 30,41	POWER	+5V VDD pins.
GND	14,16,27, 28,31,32, 33,35,36, 38,39,40	GROUND	Ground pins
SLOT0CC#	15	IN <sub>ts</sub>	CPU presence signal. 0, means CPU is present. 1, means CPU is absent.

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NC	23,26,37, 42,43,44		No connect.
SCL	21	IN <sub>ts</sub>	Serial Bus Clock.
SDA	22	I/OD <sub>8ts</sub>	Serial Bus bi-directional Data.
+3.3VIN	34	AIN	0V to 4.096V FSR Analog Inputs.
EVNTRP1-4	45-48	I/O <sub>12ts</sub>	Event trapping to selection speech output sound.





## 6. FUNCTION DESCRIPTION

### 6.1 Speech Function

#### 6.1.1 General Description

The W83791SD is a derivative of Winbond's *PowerSpeech*<sup>™</sup> synthesizers. There are up to 5 hardware trigger inputs and 128 programmable software event trigger inputs. If more than two events happen simultaneously, the priority set by the internal H/W is: SLOTOCC# > EVNTRAP1 > EVNTRAP2 > EVNTRAP3 > EVNTRAP4 > EVNTRAP5 > TRIGREG(Index 09h) 128 events. Software trigger is able to accommodate 128 event triggers, with timeout register (index 08h) enabled in advance for allowance of time on detecting devices. That is, once the system's power is on, BIOS can fill trigger event and speech voice will not be sent till the system fails owing to timeout. In addition, to prevent events from taking place simultaneously.

#### 6.1.2 Event Trigger Queue

W83791SD provides 8 byte FIFO queue to store event trigger, i.e, the first 8 event can be served by speech and speech will clear FIFO queue after service. Coding of Speech program must assign correct CPU\_MODE event vector to issue correct speech voices correspondent to speech trigger events. For example, CPU\_MODE event vector =1 represents absence of CPU, then coding speech with CPU is absent voice. When W83791SD detects no CPU exists, it will send vector = 1 to speech synthesizer and play this voice data. Following is the block diagram of the 8-Byte event trigger queue.

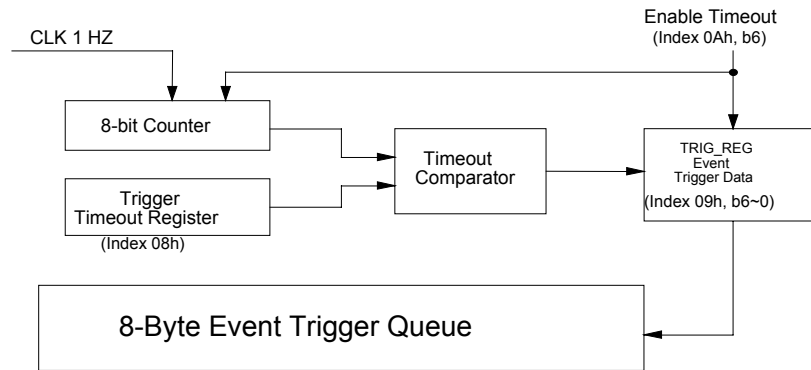


Figure 1. Event trigger Queue

For example: As BIOS usually has POST (Power On Self Test) program, then it will test every item step by step if no failure takes place, however, if it detects a failure on a specific item, it will hang on there. Therefore, BIOS could write timeout value to register 08h and start timer setup speech trigger event (register 09h), then is BIOS test program started. Whenever the system is hang on specific item such as DRAM testing, W83791SD would say "DRAM test fails" after the timeout previously set at CR[08h]. On the contrary, if DRAM test is ok, then BIOS could update the timeout value and proceed to the next test program.

Below is the speech CPU\_MODE table of W83791SD:

CPU_MODE item	Definition	Vector (H)
<b>POI</b>	Reserverd	0,32
<b>SLOTOCC</b>	CPU present or absent	1
<b>EVNTRAP1(TG1)</b>	Hardware trgger1	2
<b>EVNTRAP2</b>	Hardware trgger2	3
<b>EVNTRAP3</b>	Hardware trgger3	4
<b>EVNTRAP4</b>	Hardware trgger4	5
<b>EVNTRAP5</b>	Hardware trgger5	6
<b>TRIGREG</b>	I2C setting software trigger	80-FF

Table 1. CPU\_MODE Table

### 6.1.3 Connection of EEPROM

As is described previously that the W83791SD has connectable W55FXX to store voice data. To expand the storage capacity, users can select many W55FXX to connect with each other. The maximum capacity could be up to 16Mbit. Following is the connection chart of W55FX with W83791SD.

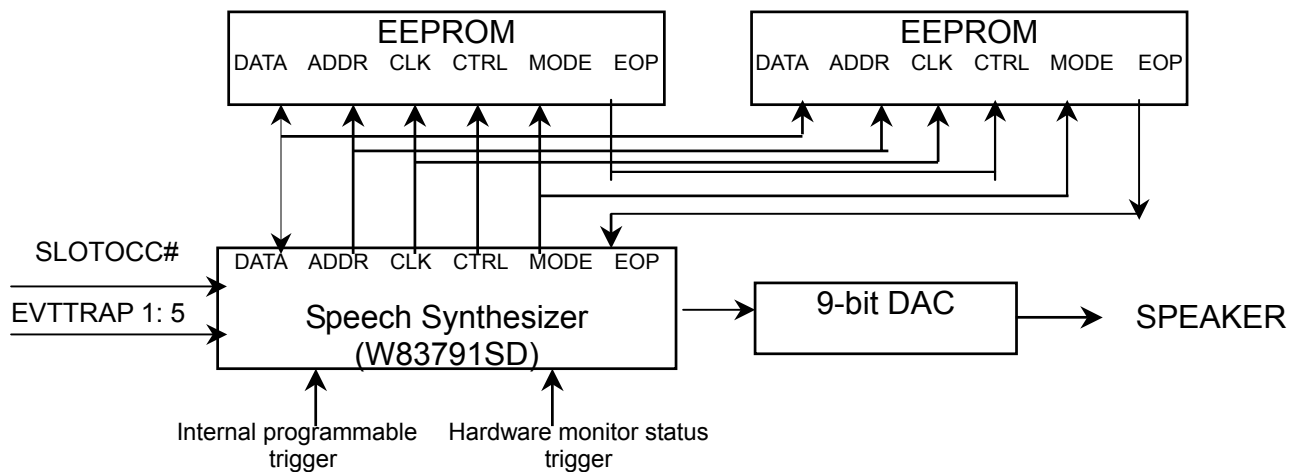


Figure 2. Speech Function Diagram

#### 6.1.4 Speaker Output

Speech output pin is a 8 bit Current D/A converter, with which loading is needed. The resistor could range from 510~1K ohm and bipolar could be a low power NPN bipolar with  $\beta$

$\Omega$ . Besides, SPK can also connect to AC97 codec chip Line\_Out.  
C is decouple capacitor and is usually 200p- 0.01uF

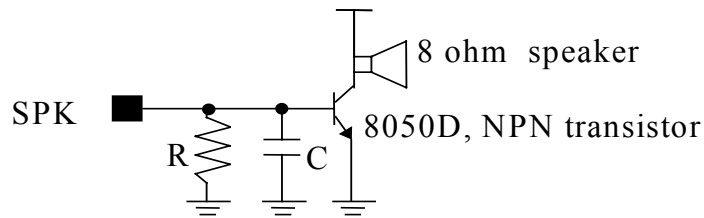


Figure. 3



## 7. ELECTRICAL CHARACTERISTICS

### 7.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 7.0	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### 7.2 DC Characteristics

(Ta = 0° C to 70° C, VDD = 5V ± 10%, VSS = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
<b>I/O<sub>12t</sub> - TTL level bi-directional pin with source-sink capability of 12 mA</b>						
Input Low Voltage	V <sub>IL</sub>			0.8	V	
Input High Voltage	V <sub>IH</sub>	2.0			V	
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 12 mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = - 12 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = V <sub>DD</sub>
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0V
<b>I/O<sub>12ts</sub> - TTL level bi-directional pin with source-sink capability of 12 mA and schmitt-trigger level input</b>						

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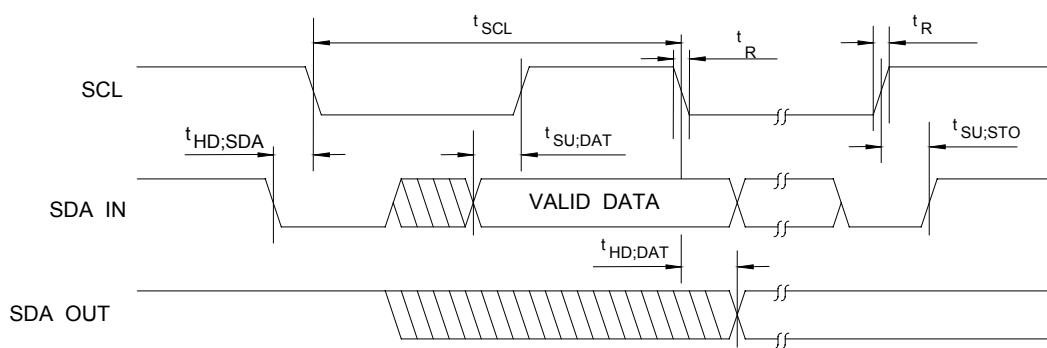
Input Low Threshold Voltage	V <sub>IL</sub>	0.5	0.8	1.1	V	V <sub>DD</sub> = 5 V
Input High Threshold Voltage	V <sub>IH</sub>	1.6	2.0	2.4	V	V <sub>DD</sub> = 5 V
Hysteresis	V <sub>TH</sub>	0.5	1.2		V	V <sub>DD</sub> = 5 V
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 12 mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = - 12 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = V <sub>DD</sub>
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0V
<b>OUT<sub>12t</sub> - TTL level output pin with source-sink capability of 12 mA</b>						
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 12 mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = -12 mA
<b>OD<sub>8</sub> - Open-drain output pin with sink capability of 8 mA</b>						
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 8 mA
<b>OD<sub>12</sub> - Open-drain output pin with sink capability of 12 mA</b>						
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 12 mA
<b>OD<sub>48</sub> - Open-drain output pin with sink capability of 48 mA</b>						
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 48 mA
<b>IN<sub>t</sub> - TTL level input pin</b>						
Input Low Voltage	V <sub>IL</sub>			0.8	V	
Input High Voltage	V <sub>IH</sub>	2.0			V	
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = V <sub>DD</sub>



Input Low Leakage	ILIL			-10	$\mu\text{A}$	$V_{\text{IN}} = 0 \text{ V}$
<b>IN<sub>ts</sub> - TTL level Schmitt-triggered input pin</b>						
Input Low Threshold Voltage	V <sub>t-</sub>	0.5	0.8	1.1	V	V <sub>DD</sub> = 5 V
Input High Threshold Voltage	V <sub>t+</sub>	1.6	2.0	2.4	V	V <sub>DD</sub> = 5 V
Hysteresis	V <sub>TH</sub>	0.5	1.2		V	V <sub>DD</sub> = 5 V
Input High Leakage	ILIH			+10	$\mu\text{A}$	$V_{\text{IN}} = V_{\text{DD}}$
Input Low Leakage	ILIL			-10	$\mu\text{A}$	$V_{\text{IN}} = 0 \text{ V}$

## 7.3 AC Characteristics

### 7.3.1 Serial Bus Timing Diagram



Serial Bus Timing Diagram

### Serial Bus Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	$t_{SCL}$	10		uS
Start condition hold time	$t_{HD;SDA}$	4.7		uS
Stop condition setup-up time	$t_{SU;STO}$	4.7		uS
DATA to SCL setup time	$t_{SU;DAT}$	120		nS
DATA to SCL hold time	$t_{HD;DAT}$	5		nS
SCL and SDA rise time	$t_R$		1.0	uS
SCL and SDA fall time	$t_F$		300	nS

## 8. HOW TO READ THE TOP MARKING

The top marking of W83791SD



Left: Winbond logo

1st line: Type number W83791SD, D means LQFP (Thickness = 1.4 mm).

2nd line: Tracking code 025 A A

025: packages made in 2000, week 25

G: assembly house ID; A means ASE, O means OSE, G means Greatek

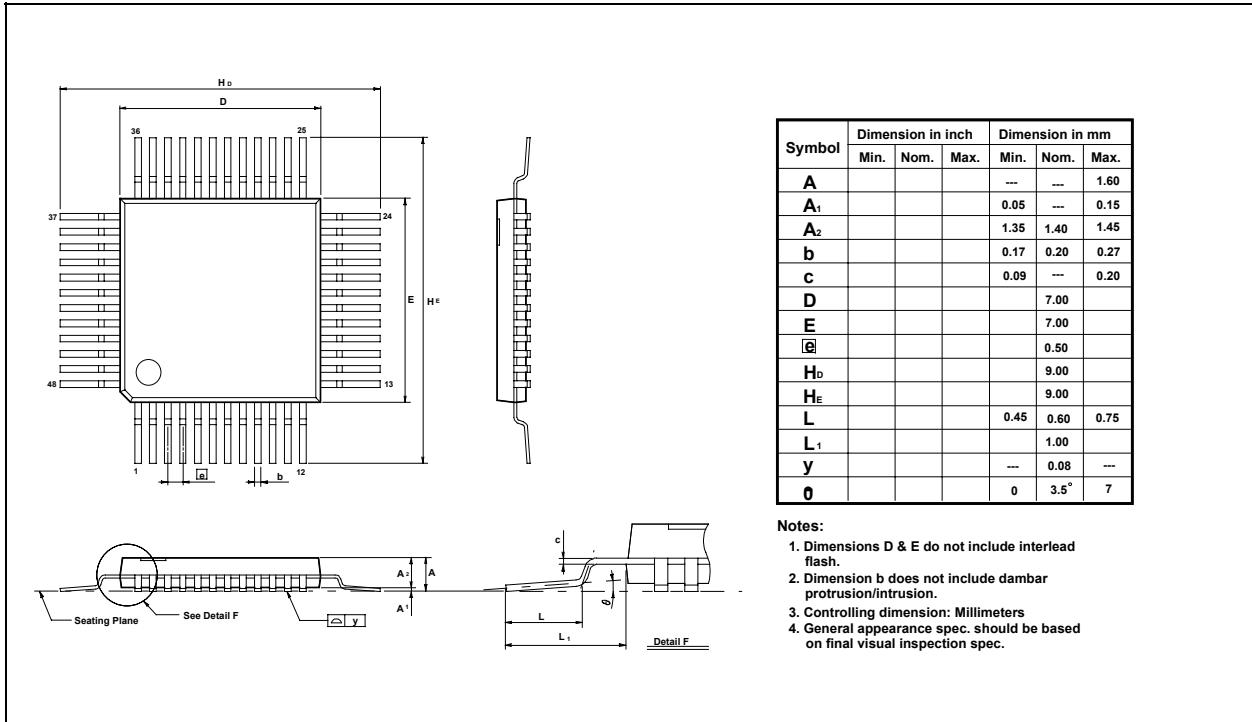
C: IC revision; A means version A, C means version C





## 9. PACKAGE SPECIFICATION

(48-pin LQFP)



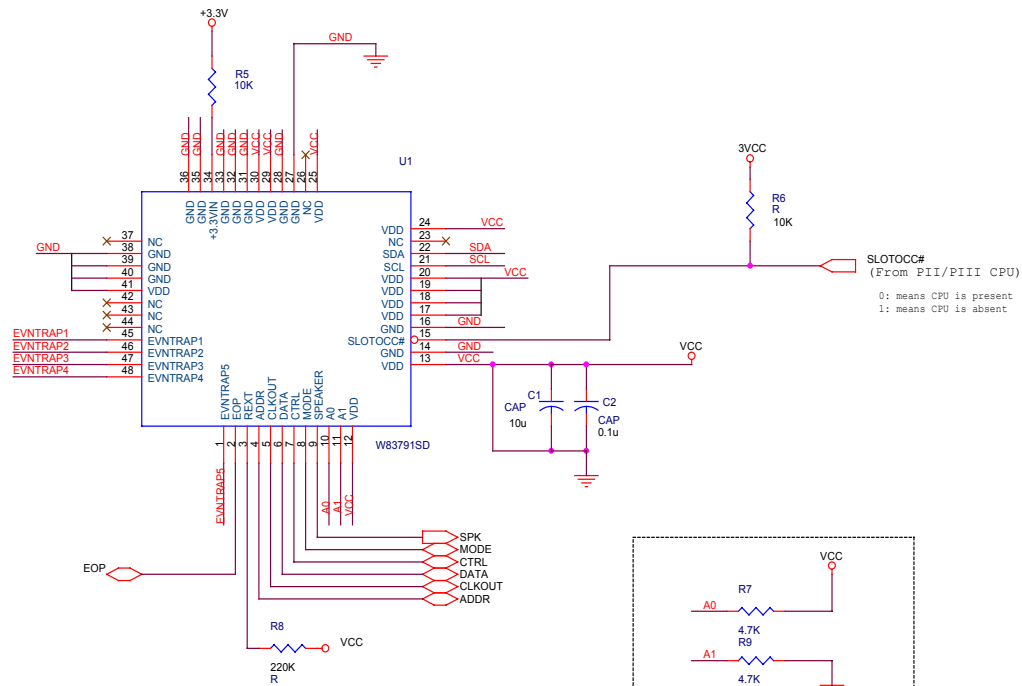
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# NOTE :

The EVNTRAP1-5 trigger inputs default are low to high active.



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REV	Description
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