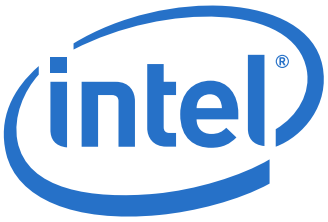

Intel Atom® Processor E3800

Specification Update

(Formerly Bay Trail -I SoC)

March 2021

Document Number: 329901-015US

Contents

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Revision History

Date	Revision	Description
March 2021	015	Issue from PCIe Card - Removed errata VLI58 SoC PCIe LTSSM May Not Enter Detect Within 20 ms.
November 2019	014	Added errata VLI96 xHCI Short Packet Event Using Non-Event Data TRB Updated Documentation Changes table. Added new section, "9.5.14 PCU - iLB - LPC DC Specification" to Documentation changes.
August 2019	013	Added Thermal Sensor, 7.2.1 RTC Power Well Transition (G5 to G3 States Transition) and 7.2.2 G3 to S0 to Documentation Changes section. Change FCBA package to FCBGA for SR1RE and SR1RD on Identification Table for Intel Atom® Processor E3800 Product Family.
April 2019	012	Updated Related Documents, Specification Clarifications, and Documentation Changes.
October 2018	011	Added Errata VLI95.
July 2018	010	Updated Errata VLI84 in "Errata Summary Table". Added Table 2, "Processor Identification by Register Content for Intel Atom Processor E3800" on page 15. Updated Errata VLI89.
May 2018	009	Added extra column D-1 under Steppings for Errata Summary Table. Update no.12 under Documentation Changes.
March 2018	008	Updated link under Related Documents.
January 2018	007	Updated Errata summary table. Specification Change Table updated. Documentation Change Table updated. Added Identification information and Component marking sections. Erratum VLI5 removed. Erratum VLI55 revised title. Added Erratum VLI93 and VLI94. Specification Changes - Removed item 6. PCU - SPI NOR AC Specifications. Documentation Changes section updated.
November 2017	006	Updated Errata VLI77. Added Table 141 and 171 for Specification Changes. Updated Documentation Changes no.12.
October 2017	005	Updated Related documents table. Updated Errata Summary Table. Added Errata VLI91 and VLI92. Updates Specification Changes Table. Updated Documentation Changes no.5 through no. 10. Added Specification Change #5.
August 2017	004	Added Errata VLI90.
July 2017	003	Added Errata VLI89. Updated Tables and sections for Documentation Changes and Specification Changes
February 2016	002	Revised Related Documents table. Added Errata VLI8 and VLI9, VLI62 through VLI88. Removed all VLI1S through VLI4S. Added Tables and sections for Specification Changes, Specification Clarifications, and Documentation Changes.
October 2013	001	Initial Release.

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Preface

The Affected Documents is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this document and are no longer published in other documents. This document may also contain information that has not been previously published.

Throughout this document Intel Atom® Processor E3800 Product Family is referred as Processor or SoC.

Affected Documents

Document Title	Document Number/ Location
Intel Atom® Processor E3800 Product Family Datasheet	538136

Note: Contact local Intel representative for the latest document number.

Related Documents

Document Title	Document Number/ Location[1]
Intel® 64 and IA-32 Architectures Software Developer's Manual Combined, Document Number 325462	https://software.intel.com/en-us/articles/intel-sdm
Intel® 64 and IA-32 Intel Architecture Optimization Reference Manual, Document Number 248966	
Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes, Document Number 252046	

Note: Documentation changes for Intel® 64 and IA-32 Architecture Software Developer's Manual, and bug fixes are posted in the Intel® 64 and IA-32 Architecture Software Developer's Manual Documentation Changes.

Nomenclature

Errata are design defects or errors. These may cause the SoC behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

S-Spec Number is a five-digit code used to identify products. Products are differentiated by their unique characteristics, for example, core speed, L2 cache size, package type, etc. as described in the component identification information table. Read all notes associated with each S-Spec number.

QDF Number is a four-digit code used to distinguish between engineering samples. These samples are used for qualification and early design validation. The functionality of these parts can range from mechanical only to fully functional. This document has a component identification information table that lists these QDF numbers and the corresponding product details.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

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Errata Summary

The table included in this section indicated the Errata that apply to the Intel Atom® Processor E3800 Product Family. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exist in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of a table row indicates this erratum is either new or modified from the previous version of the document.

Errata Summary Table

Number	Stepping				Status	Errata Title
	B-2	B-3	D-0	D-1		
VLI1	X	X	X	X	No Fix	Accessing Unimplemented ISP MMIO Space May Cause a System Hang
VLI2	X	X	X	X	No Fix	Quad Word Transactions in Violation of Programming Model May Result in System Hang
VLI3	X	X	X	X	No Fix	GPIO Registers Do Not Support 8 or 16-bit Transactions
VLI4	X	X	X	X	No Fix	CSI Interface May Not Correct Certain Single bit Errors
VLI5						Removed. Duplicate of VLI80
VLI6	X	X	X	X	No Fix	Anomalies in USB xHCI PME Enable and PME Status
VLI7	X	X	X	X	No Fix	eMMC Asynchronous Abort May Cause a Hang
VLI8	X	X	X	X	No Fix	USB xHCI SuperSpeed Packet with Invalid Type Field Issue
VLI9	X	X	X	X	No Fix	USB xHCI Behavior with Three Consecutive Failed U3 Entry Attempts
VLI10	X	X	X	X	No Fix	SD Host Controller Incorrectly Reports Supporting of Suspend/ Resume Feature
VLI11	X	X	X	X	No Fix	SD Host Controller Error Status Registers May be Incorrectly Set
VLI12	X	X	X	X	No Fix	SD Host Controller Registers Are Not Cleared by Software Reset
VLI13	X	X	X	X	No Fix	Timing Specification Violation on SD Card Interface
VLI14	X	X	X	X	No Fix	SD Card Controller Does Not Disable Clock during Card Power Down
VLI15	X	X	X	X	No Fix	Reset Sequence May Take Longer Than Expected When ACG is Enabled in SD and SDIO Controllers
VLI16	X	X	X	X	No Fix	XHCI Port Assigned Highest SlotID When Resuming from Sx Issue
VLI17	X	X	X	X	No Fix	LFPS Detect Threshold
VLI18	X	X	X	X	No Fix	Set Latency Tolerance Value Command Completion Event Issue
VLI19	X	X	X	X	No Fix	xHCI Data Packet Header and Payload Mismatch Error Condition
VLI20	X	X	X	X	No Fix	USB xHCI Max Packet Size and Transfer Descriptor Length Mismatch
VLI21	X	X	X	X	No Fix	USB EHCI RMH Port Disabled Due to Device Initiated Remote Wake

Number	Stepping				Status	Errata Title
	B-2	B-3	D-0	D-1		
VLI22	X	X	X	X	No Fix	USB EHCI Isoch in Transfer Error Issue
VLI23	X	X	X	X	No Fix	USB EHCI Babble Detected with SW Overscheduling
VLI24	X	X	X	X	No Fix	USB EHCI Full-/low-speed EOP Issue
VLI25	X	X	X	X	No Fix	USB EHCI Asynchronous Retries Prioritized Over Periodic Transfers
VLI26	X	X	X	X	No Fix	USB EHCI FS/LS Incorrect Number of Retries
VLI27	X	X	X	X	No Fix	USB EHCI RMH Think Time Issue
VLI28	X	X	X	X	No Fix	USB EHCI Full-/low-speed Device Removal Issue
VLI29	X	X	X	X	No Fix	Reported Memory Type May Not Be Used to Access the VMCS and Referenced Data Structures
VLI30	X	X	X	X	No Fix	A Page Fault May Not be Generated When the PS bit is set to "1" in a PML4E or PDPTE
VLI31	X	X	X	X	No Fix	CS Limit Violations May Not be detected after VM Entry
VLI32	X	X	X	X	No Fix	IA32_DEBUGCTL.FREEZE_PERFMON_ON_PMI is Incorrectly Cleared by SMI
VLI33	X	X	X	X	No Fix	PEBS Record EventingIP Field May be Incorrect after CS.Base Change
VLI34	X	X	X	X	No Fix	Some Performance Counter Overflows May Not be logged in IA32_PERF_GLOBAL_STATUS When FREEZE_PERFMON_ON_PMI is enabled
VLI35	X	X	X	X	No Fix	MOVNTDQA from WC Memory May Pass Earlier Locked Instructions
VLI36	X	X	X	X	No Fix	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
VLI37	X	X	X	X	No Fix	SDIO Host Controller Does Not Control the SDIO Bus Power
VLI38	X	X	X	X	No Fix	USB HSIC Ports Incorrectly Reported as Removable
VLI39	X	X	–	–	Fixed	Multiple Threads That Access the ISP Concurrently May Lead to a System Hang
VLI40	X	X	X	X	No Fix	Premature Asynchronous Interrupt Enabling May Lead to Loss of SDIO Wi-Fi Functionality
VLI41	X	X	X	X	No Fix	Paging Structure Entry May be Used Before Accessed And Dirty Flags Are Updated
VLI42	X	X	X	X	No Fix	Certain eMMC Host Controller Registers Are Not Cleared by Software Reset

Number	Stepping				Status	Errata Title
	B-2	B-3	D-0	D-1		
VLI43	X	X	X	X	No Fix	LPE audio output not available on HDMI when HDAudio Controller is disabled
VLI44	X	X	X	X	No Fix	USB Device Mode Controller May Not Successfully Switch to High-Speed Data Rate
VLI45	X	X	X	X	No Fix	USB Device Mode Controller Response Time May Exceed The Specification
VLI46	X	X	X	X	No Fix	USB Device Mode Controller May Not Enter the SS.Inactive State
VLI47	X	X	X	X	No Fix	USB EHCI Full-/Low-speed Port Reset or Clear TT Buffer Request
VLI48	X	X	X	X	No Fix	USB Device Mode Controller LFPS Transmission Period Does Not Meet USB 3.0 Specification
VLI49	X	X	X	X	No Fix	Performance Monitor Instructions Retired Event May Not Count Consistently
VLI50	X	X	X	X	No Fix	MTF VM Exit May be Delayed Following a VM Entry That Injects a Software Interrupt
VLI51	X	X	X	X	No Fix	LBR Stack And Performance Counter Freeze on PMI May Not Function Correctly
VLI52	X	X	X	X	No Fix	Certain MIPI CSI Sensors May Not Operate Correctly At Low Clock Frequencies
VLI53	X	X	X	X	No Fix	USB Legacy Support SMI Not Available from xHCI Controller
VLI54	X	X	X	X	No Fix	SD Card UHS-I Mode is Not Fully Supported
VLI55	-	-	-	-	Fixed	EOI Transactions May Not be Sent if Software Enters Core C6 During an Interrupt Service Routine - REMOVED
VLI56	X	X	X	X	No Fix	USB xHCI May Execute a Stale Transfer Request Block (TRB)
VLI57	X	X	X	X	No Fix	HD Audio Recording And Playback May Glitch or Stop
VLI58	X	X	X	X	No Fix	This erratum has been removed.
VLI59	X	X	X	X	No Fix	SATA Signal Voltage Level Violation
VLI60	X	X	X	X	No Fix	PCIe Root Ports Unsupported Request Completion
VLI61	X	X	X	X	No Fix	VGA Max Luminance Voltage May Exceed VESA Limits
VLI62	X	X	X	X	No Fix	SD Card Initialization Sequence May Fail When ACG is Enabled in SD Controller
VLI63	X	X	–	–	Fixed	Reset Sequence May Not Complete Under Certain Conditions

Number	Stepping				Status	Errata Title
	B-2	B-3	D-0	D-1		
VLI64	X	X	X	X	No Fix	Multiple Drivers That Access the GPIO Registers Concurrently May Result in Unpredictable System Behavior
VLI65	X	X	X	X	No Fix	Boot May Not Complete When SMI Occurs during Boot
VLI66	X	X	X	X	No Fix	Interrupts That Target an APIC That is Being Disabled May Result in a System Hang
VLI67	X	X	X	X	No Fix	Corrected or Uncorrected L2 Cache Machine Check Errors May Log Incorrect Address in IA32_MCi_ADDR
VLI68	X	X	X	X	No Fix	Software-initiated Partition Reset May Cause a System Hang
VLI69	X	X	X	X	No Fix	Write-1-Clear Bits in PMC Registers May be Unexpectedly Cleared
VLI70	X	X	X	X	No Fix	Port Reset on USB2 Port0 And Port1 May Cause a Reset on HSIC Port0 and Port1 Respectively
VLI71	X	X	X	X	No Fix	Frequency Reported by CPUID Instruction May Not Match Published Frequency
VLI72	X	X	X	X	No Fix	Some USB Controller Capability Registers May Be Invalid After S3 Resume
VLI73	X	X	X	X	No Fix	Machine Check Status Overflow Bit May Not be Set
VLI74	X	X	X	X	No Fix	Attempts to Clear Performance Counter Overflow Bits May Not Succeed
VLI75	X	X	X	X	No Fix	SMI in 64-bit Mode May Store an Incorrect RIP to SMRAM When CS has a Non-Zero Base
VLI76	X	X	X	X	No Fix	VM Exit May Set IA32_EFER.NXE When IA32_MISC_ENABLE Bit 34 is Set to 1
VLI77	X	X	X	X	No Fix	Top Swap Mechanism May Become Incorrectly Configured
VLI78	X	X	X	X	No Fix	Certain Peripheral I/O Controllers May Hang After an Unexpectedly Long Latency Memory Transaction
VLI79	X	X	X	X	No Fix	Disabling SDIO or SDCARD May Lead To a System Hang
VLI80	X	X	–	–	Fixed	ULPI Bus Marginality for USB Device Mode
VLI81	X	X	X	X	No Fix	TLB Entries May Not Be Invalidated Properly When Bit 8 Is Set in EPT Paging-Structure Entries
VLI82	X	X	X	X	No Fix	CPUID Instruction Leaf 0AH May Return an Unexpected Value
VLI83	X	X	X	X	No Fix	Video And/or Audio Artifact May Occur When Changing Frequencies
VLI84	X	X	X	-	Fixed	USB Device May Not be Detected at System Power-On

Number	Stepping				Status	Errata Title
	B-2	B-3	D-0	D-1		
VLI85	X	X	X	X	No Fix	VM Exits During Execution of INTn in Virtual-8086 Mode with Virtual-Mode Extensions May Save RFLAGS Incorrectly
VLI86	X	X	X	X	No Fix	Clearing IA32_MC0_CTL[5] May Prevent Machine Check Notification
VLI87	X	X	X	X	No Fix	System May Unexpectedly Reboot After Shutdown
VLI88	X	X	X	X	No Fix	Unusual waveform on SATA GEN1 (1.5 Gbps) during window loading
VLI89	X	X	X	-	Fixed	System May Experience Inability to Boot or May Cease Operation
VLI90	X	X	X	X	No Fix	LPC Clock Control Using the ILB_LPC_CLKRUN# Signal May Not Behave As Expected
VLI91	X	X	X	X	No Fix	xHCI Host Controller Reset May Cause a System Hang
VLI92	X	X	-	-	Fixed	Shutdown May Occur When Memory Subsystem Signals a Machine Check Exception
VLI93	X	X	X	X	No Fix	LPE Audio Playback May Result in System Hang
VLI94	X	X	X	X	No Fix	Transient SATA Gen 1 Signal Anomaly During OS Boot
VLI95	X	X	X	X	No Fix	eMMC CRC Detection
VLI96	X	X	X	X	No Fix	xHCI Short Packet Event Using Non-Event Data TRB

Specification Changes

Number	SPECIFICATION CHANGES
1	Top Swap Feature
2	TCO Timer Clock Period
3	PCI Express Non-Common/Asynchronous Reference Clock Support
4	S4/S5 to S0 (Power Up) Sequence Specification Change
5	Table 141. The setup of PCU_SPI_MISO with respect to serial clock falling edge at the host (t184) in PCU-SPI NOR AC Specification updates
6	Table 171. Hardware Accelerated Video Decode Codec Support

Specification Clarifications

Number	SPECIFICATION CLARIFICATIONS
1	GPU Frequency Encoding Description
2	ECC Error Reporting Description
3	S4/S5 to S0 (Power Up) Sequence

Documentation Changes

Number	DOCUMENTATION CHANGES
1	Statement of Volatility (SOV)
2	ILB_RTC_TEST# and ILB_RTC_RST# RC Time Delay Calculation Formula
3	eMMC* 5.0 Functional Backward Compatibility Support Notes
4	Remove PCU- SPI AC Specification Section
5	Start Address and End Address Corrections for High Precision Event Timer (HPET)
6	CPU Base Clock (BCLK) Frequency
7	1.4.2 Intel Atom® Processor E3800 Product Family - Datasheet, Document# 538136, Section 9.6.22 PCU -iLB - LPC AC specification, Table 144 correction.
8	Thermal Sensor
9	7.2.1 RTC Power Well Transition (G5 to G3 States Transition)
10	7.2.2 G3 to S0
11	9.5.14 PCU – iLB – LPC DC Specification

This document reports Erratum are for the Intel Atom® Processor E3800 Product Family. Customers can use this data to understand the current issues that Intel is investigating.

An Erratum that is correlated to the Intel Atom® Processor E3800 Product Family silicon and classified as "no fix" will be migrated to the Intel Atom® Processor E3800 Product Family Specification Update as an Erratum.

Intel will continue to update customers on Errata as progress is made. Notify your Intel representative if you encounter similar problems. The Intel Atom® Processor E3800 Product Family Errata report numbering method may not be sequential since many internal Errata are quickly root caused and are thus not disclosed in the Errata Report. Others are determined to not be actual problems either because they are duplicates, they are particular to Intel's testing environment, or they are testing errors.

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Identification Information

Intel Atom® Processor E3800 Product Family on 22-nm process stepping can be identified by the register contents in Errata Summary Table.

When EAX is initialized to a value of 1, the CPUID instruction returns the Extended Family, Extended Model, Type, Family, Model and Stepping value in the EAX register. Note that the EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

Table 1. Component Identification via Programming Interface

Reserved	Extended Family[1]	Extended Model[2]	Reserved	Processor Type[3]	Family Code[4]	Model Number[5]	Stepping ID[6,7]
31:28	27:20	19:16	15:13	12	11	7:4	3:0
0000b	0000000b	0011b	000b	0b	0110b	111b	A0: 0001b B0: 0010b B2: 0011b B3: 0011b D0: 1001b D1: 1001b

Notes:

1. The Extended Family, bits [27:20] are used in conjunction with the Family Code, specified in bits [11:8], to indicate whether the processor belongs to the Intel386®, Intel486®, Pentium®, Pentium Pro, Pentium 4, or Intel Core processor family.
2. The Extended Model, bits [19:16] in conjunction with the Model Number, specified in bits [7:4], are used to identify the model of the processor within the processor's family.
3. The Processor Type, specified in bits [13:12] indicates whether the processor is an original OEM processor, an OverDrive processor, or a dual processor (capable of being used in a dual processor system).
4. The Family Code corresponds to bits [11:8] of the EDX register after RESET, bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
5. The Model Number corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
6. The Stepping ID in bits [3:0] indicates the revision number of that model. See Identification Table for Intel Atom® Processor E3800 Product Family for the processor stepping ID number in the CPUID information.
7. D0 and D1 Steppings can be differentiated by reading the Manufacturer ID (PCIE_REG_MANUFACTURER_ID) register field - [B:0, D:31, F:0, Offset:F8h, Bits 23:16]. D0 stepping processors will have a value of 11h and D1 stepping processors will have a value of 13h.

Table 2. Processor Identification by Register Content for Intel Atom Processor E3800

Stepping	Vendor ID[1]	Platform ID[2]	Host Device ID[3]	Revision ID[4]
B2	8086h	0h	F00h	0Ah
B3	8086h	0h	F00h	0Ch
D0	8086h	0h	F00h	11h
D1	8086h	0h	F00h	11h

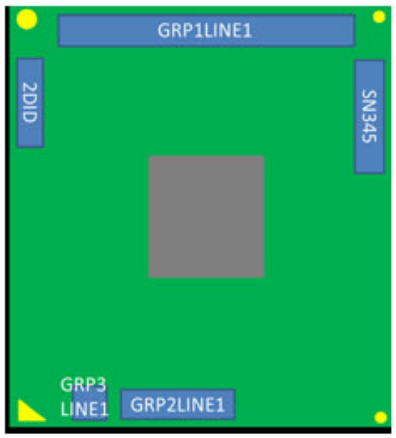
Notes:

1. The Vendor ID corresponds to bits 15:0 of the CUNIT_REG_DEVICEID register located at offset 0h in the PCI device 0, Function 0 configuration space.
2. The Platform ID corresponds to bits 52:50 of the IA32_PLATFORM_ID MSR located at offset 17h.
3. The Host Device ID corresponds to bits 31:16 of the CUNIT_REG_DEVICEID register located at offset 0h in the PCI Device 0, Function 0 configuration space.
4. The Revision Number corresponds to bits 7:0 of the CUNIT_CFG_REG_CLASSCODE register located at the offset 08h in the PCI function 0 configuration space.

Component Marking Information

Intel Atom® Processor E3800 Product Family is identified by the following component markings.

Figure 1. Intel Atom® Processor E3800 Product Family Markings



SAMPLE MARKING INFORMATION:
GRP1LINE1: i{M}{C}YY_FPO12345
GRP2LINE1: QDF /SSPEC
GRP3LINE1: {E1}

Identification Table for Intel Atom® Processor E3800 Product Family

SSPEC Number	Product Stepping	Processor #	CPUID	Max Core Speed (GHz)	Package	CPU L2 Cache Size (kB)
SR1RE	B3	E3845	30673	1.91	FCBGA	2X1024
SR1RD	B3	E3827	30673	1.75	FCBGA	2X512
SR1RC	B3	E3826	30673	1.46	FCBGA	2X512
SR1RB	B3	E3825	30673	1.33	FCBGA	2X512
SR1RA	B3	E3815	30673	1.45	FCBGA	1X512
SR1X6	D0	E3845	30679	1.91	FCBGA	2X1024
SR1X7	D0	E3827	30679	1.75	FCBGA	2X512
SR1X8	D0	E3826	30679	1.46	FCBGA	2X512
SR1X9	D0	E3825	30679	1.33	FCBGA	2X512
SR1XA	D0	E3815	30679	1.46	FCBGA	1X512
SR20Y	D0	E3805	30679	1.33	FCBGA	2X512
SR3UT	D1	E3845	30679	1.91	FCBGA	2x1024
SR3UV	D1	E3827	30679	1.75	FCBGA	2x512
SR3UX	D1	E3826	30679	1.46	FCBGA	2x512
SR3UZ	D1	E3825	30679	1.33	FCBGA	2x512

SSPEC Number	Product Stepping	Processor #	CPUID	Max Core Speed (GHz)	Package	CPU L2 Cache Size (kB)
SR3V1	D1	E3815	30679	1.46	FCBGA	1x512
SR3V3	D1	E3805	30679	1.33	FCBGA	2x512

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Errata

VLI1 Accessing Unimplemented ISP MMIO Space May Cause a System Hang

Problem: Access to unimplemented ISP (Image Signal Processor) registers should result in a software error. Due to this erratum, the transaction may not complete.

Implication: When this erratum occurs, the system may hang.

Workaround: Do not access unimplemented ISP MMIO space.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI2 Quad Word Transactions in Violation of Programming Model May Result in System Hang

Problem: Quad word (64-bit data) transactions to access two adjacent 32-bit registers of SoC internal devices may cause system hang.

Implication: Due to this erratum, violations of a device programming model may result in a hang instead of a fatal Target Abort / Completer Abort error. Software written in compliance to correct programming model will not be affected.

Workaround: Software must be written and compiled in compliance to correct programming model.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI3 GPIO Registers Do Not Support 8 or 16-bit Transactions

Problem: Due to this erratum, only aligned DWord accesses to GPIO registers function correctly. This erratum applies to GPIO registers whether in MMIO space or IO space.

Implication: GPIO register transactions using byte or word accesses or unaligned DWord accesses will not work correctly.

Workaround: Always use aligned 32-bit transactions when accessing GPIO registers.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI4 CSI Interface May Not Correct Certain Single bit Errors

Problem: The CSI (Camera Serial Interface) ECC (Error Correcting Code) implementation may not correctly handle single-bit errors in the ECC field and may incorrectly flag as double-bit errors.

Implication: Due to this erratum, some single-bit errors may be treated as double-bit errors. Intel has not observed this erratum with any commercially available software or system.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI5 Removed. Duplicate of VLI80

VLI6 Anomalies in USB xHCI PME Enable and PME Status

Problem: The PME_En (bit 8) and PME_Status (bit 15) in xHCI's PCI PMCSR (Bus 0, Device 20, Function 0, Offset 0x74) do not comply with the PCI specification.

Implication: If a standard bus driver model for this register is applied, wake issues and system slowness may happen.

Workaround: Use Intel-provided BIOS ASL code or refer to Intel-provided xHCI driver reference code.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI7 eMMC Asynchronous Abort May Cause a Hang

Problem: Use of an Asynchronous Abort command to recover from an eMMC transfer error or use of a high priority interrupt STOP_TRANSMISSION command may result in a hang.

Implication: Using Asynchronous Abort command may cause a hang. Intel has not observed this erratum to impact the operation of any commercially available system.

Workaround: The eMMC driver should use High Priority Interrupt SEND_STATUS mode per JEDEC STANDARD eMMC, version 4.5. A minimum wait time of 128us between getting an error interrupt and issuing a software reset will avoid this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI8 USB xHCI SuperSpeed Packet with Invalid Type Field Issue

Problem: If the encoding for the "type" field for a SuperSpeed packet is set to a reserved value and the encoding for the "subtype" field is set to "ACK", the xHCI may accept the packet as a valid acknowledgment transaction packet instead of ignoring the packet.

Note: The USB 3.0 specification requires that a device never set any defined fields to reserved values.

Implication: System implication depends on the misbehaving device and may result in anomalous system behavior.

Note: This issue has only been observed in a synthetic test environment with a synthetic device.

Workaround: None identified

Status: For the steppings affected, see the Summary Tables of Changes.

VLI9 USB xHCI Behavior with Three Consecutive Failed U3 Entry Attempts

Problem: The xHCI does not transition to the SS.Inactive USB 3.0 LTSSM (Link Training and Status State Machine) state after a SuperSpeed device fails to enter U3 upon three consecutive attempts.

Note: The USB 3.0 specification requires a SuperSpeed device to enter U3 when directed.

Implication: The xHCI will continue to try to initiate U3. The implication is driver and operating system dependent.

Workaround: None identified

Status: For the steppings affected, see the Summary Tables of Changes.

VLI10 SD Host Controller Incorrectly Reports Supporting of Suspend/ Resume Feature

Problem: SDIO, SD Card, and eMMC Controllers should not indicate the support of optional Suspend/Resume feature documented in the SD Host Controller Standard Specification Version 3.0. Due to this erratum, the default value in the Capabilities Register (offset 040H) incorrectly indicates to the software that this feature is supported.

Implication: If software utilizes the Suspend/Resume feature, data may not be correctly transferred between memory and SD device.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI11 SD Host Controller Error Status Registers May be Incorrectly Set

Problem: This erratum impacts SDIO, SD Card, and eMMC SD Host Controllers. Auto CMD Error Status Register (offset 03CH, Bits [7:1]) may be incorrectly set for software-issued commands (for example: CMD13) that generate errors when issued close to the transmission of an Auto CMD12 command. In addition, the Error Interrupt Status Register Bits (offset 032H) are similarly affected.

Implication: Software may not be able to interpret SD Host controller error status.

Workaround: Software should follow the same error recovery flow whenever an error status bit is set. Alternatively, don't use software-issued commands that have Auto CMD12 enabled.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI12 SD Host Controller Registers Are Not Cleared by Software Reset

Problem: This erratum impacts SDIO, SD Card, and eMMC SD Host Controllers. When Software Reset is asserted, registers such as SDMA System Address / Argument 2 (offset 00H) in SD Host Controller are not cleared, failing to comply with the SD Host Controller Specification 3.0.

Implication: Intel has not observed this erratum to impact any commercially available software.

Workaround: Driver is expected to reprogram these registers before issuing a new command.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI13 Timing Specification Violation on SD Card Interface

Problem: SD Card interface IO circuitry is not optimized for platform conditions during operation at 3.3 V.

Implication: Due to this erratum, there is an increased risk of a transfer error.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI14 SD Card Controller Does Not Disable Clock during Card Power Down

Problem: The clock and power control of the SD card controller are not linked. Therefore, the SD card controller does not automatically disable the SD card clock when the SD card power is disabled.

Implication: When an SD card is inserted into the system and powered off, the clock to the SD card will continue to be driven. Although this behavior is common, it is a violation of the SD Card Spec 3.0.

Workaround: To address this problem, the SD card clock should be enabled/disabled in conjunction with SD card power.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI15 Reset Sequence May Take Longer Than Expected When ACG is Enabled in SD and SDIO Controllers

Problem: When ACG (Auto Clock Gating) is enabled in SD and SDIO controllers, the reset sequence may take longer than expected, possibly resulting in a software timeout.

Implication: Due to this erratum, a longer response time may be observed after a software-initiated controller reset.

Workaround: A BIOS workaround has been identified. Refer to the latest version of "Bay Trail–M/D SoC BIOS Writers Guide."

Status: For the steppings affected, see the Summary Tables of Changes.

VLI16 XHCI Port Assigned Highest SlotID When Resuming from Sx Issue

Problem: If a device is attached while the platform is in S3 or S4 and the device is assigned the highest assignable Slot ID upon resume, the xHCI may attempt to access an unassigned main memory address.

Implication: Accessing unassigned main memory address may cause a system software timeout leading to possible system hang.

Workaround: System SW can detect the timeout and perform a host controller reset prior to avoid a system hang.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI17 LFPS Detect Threshold

Problem: The USB 3.0 host and device controllers' LFPS (Low Frequency Periodic Signal) detect threshold is higher than the USB 3.0 specification maximum of 300 mV.

Implication: The USB 3.0 host and device controllers may not recognize LFPS from SuperSpeed devices transmitting at the minimum low-power peak-to-peak differential voltage (400 mV) as defined by USB 3.0 specification for the optional capability for Low-Power swing mode. Intel has not observed this erratum to impact the operation of any commercially available system.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI18 Set Latency Tolerance Value Command Completion Event Issue

Problem: The xHCI controller does not return a value of '0' for slot ID in the command completion event TRB (Transfer Request Block) for a set latency tolerance value command.

Note: This violates the command completion event TRB description in section 6.4.2.2 of the eXtensible Host Controller Interface for Universal Serial Bus (xHCI) specification, revision 1.0.

Implication: There are no known functional failures due to this issue.

Note: Set latency tolerance value command is specific to the controller and not the slot. Software knows which command was issued and which fields are valid to check for the event.

Note: xHCI CV compliance test suite: Test TD4.10: Set Latency Tolerance Value Command Test may issue a warning.

Workaround: None identified

Status: For the steppings affected, see the Summary Tables of Changes.

VLI19 xHCI Data Packet Header and Payload Mismatch Error Condition

Problem: If a SuperSpeed device sends a DPH (Data Packet Header) to the xHCI with a data length field that specifies less data than is actually sent in the DPP (Data Packet Payload), the xHCI will accept the packet instead of discarding the packet as invalid.

Note: The USB 3.0 specification requires a device to send a DPP matching the amount of data specified by the DPH.

Implication: The amount of data specified in the DPH will be accepted by the xHCI and the remaining data will be discarded and may result in anomalous system behavior.

Note: This issue has only been observed in a synthetic test environment with a synthetic device.

Workaround: None identified

Status: For the steppings affected, see the Summary Tables of Changes.

VLI20 USB xHCI Max Packet Size and Transfer Descriptor Length Mismatch

Problem: The xHCI may incorrectly handle a request from a low-speed or full-speed device when all the following conditions are true:

- The sum of the packet fragments equals the length specified by the TD (Transfer Descriptor)
- The TD length is less than the MPS (Max Packet Size) for the device
- The last packet received in the transfer is "0" or babble bytes

Implication: The xHCI will halt the endpoint if all the above conditions are met. All functions associated with the endpoint will stop functioning until the device is unplugged and reinserted.

Workaround: None identified

Status: For the steppings affected, see the Summary Tables of Changes.

VLI21 USB EHCI RMH Port Disabled Due to Device Initiated Remote Wake

Problem: During resume from Global Suspend, the RMH controller may not send SOF soon enough to prevent a device from entering suspend again. A collision on the port may occur if a device initiated remote wake occurs before the RMH controller sends SOF.

Note: Intel has only observed this issue when two USB devices on the same RMH controller send remote wake within 30 ms window while RMH controller is resuming from Global Suspend

Implication: The RMH host controller may detect the collision as babble and disable the port.

Workaround: Intel recommends system software to check bit 3 (Port Enable/Disable Change) together with bit 7 (Suspend) of Port N Status and Control PORTC registers when determining which port(s) have initiated remote wake. Intel recommends the use of the USB xHCI controller which is not affected by this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI22 USB EHCI Isoch in Transfer Error Issue

Problem: If a USB full-speed inbound isochronous transaction with a packet length 190 bytes or greater is started near the end of a microframe the SoC may see more than 189 bytes in the next microframe.

Implication: If the SoC sees more than 189 bytes for a microframe an error will be sent to software and the isochronous transfer will be lost. If a single data packet is lost no perceptible impact for the end user is expected.

Note: Intel has only observed the issue in a synthetic test environment where precise control of packet scheduling is available, and has not observed this failure in its compatibility validation testing.

- Isochronous traffic is periodic and cannot be retried thus it is considered good practice for software to schedule isochronous transactions to start at the beginning of a microframe. Known software solutions follow this practice.
- To sensitize the system to the issue additional traffic such as other isochronous transactions or retries of asynchronous transactions would be required to push the inbound isochronous transaction to the end of the microframe.

Workaround: Intel recommends the use of the USB xHCI controller which is not affected by this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI23 USB EHCI Babble Detected with SW Overscheduling

Problem: If software violates USB periodic scheduling rules for full-speed isochronous traffic by overscheduling, the RMH may not handle the error condition properly and return a completion split with more data than the length expected.

Implication: If the RMH returns more data than expected, the endpoint will detect packet babble for that transaction and the packet will be dropped. Since overscheduling occurred to create the error condition, the packet would be dropped regardless of RMH behavior. If a single isochronous data packet is lost, no perceptible impact to the end user is expected.

Note: USB software overscheduling occurs when the amount of data scheduled for a microframe exceeds the maximum budget. This is an error condition that violates the USB periodic scheduling rule.

Note: This failure has only been recreated synthetically with USB software intentionally overscheduling traffic to hit the error condition.

Workaround: Intel recommends the use of the USB xHCI controller which is not affected by this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI24 USB EHCI Full-/low-speed EOP Issue

Problem: If the EOP of the last packet in a USB Isochronous split transaction (Transaction >189 bytes) is dropped or delayed 3 ms or longer the following may occur:

- If there are no other pending low-speed or full-speed transactions the RMH will not send SOF, or Keep-Alive. Devices connected to the RMH will interpret this condition as idle and will enter suspend.
- If there is other pending low-speed or full-speed transactions, the RMH will drop the isochronous transaction and resume normal operation.

Implication: If there are no other transactions pending, the RMH is unaware a device has entered suspend and may start sending a transaction without waking the device. The implication is device dependent, but a device may stall and require a reset to resume functionality. If there are other transactions present, only the initial isochronous transaction may be lost. The loss of a single isochronous transaction may not result in end user perceptible impact.

Note: Intel has only observed this failure when using software that does not comply with the USB specification and violates the hardware isochronous scheduling threshold by terminating transactions that are already in progress.

Workaround: Intel recommends the use of the USB xHCI controller which is not affected by this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI25 USB EHCI Asynchronous Retries Prioritized Over Periodic Transfers

Problem: The integrated USB RMH incorrectly prioritizes full-speed and low-speed asynchronous retries over dispatchable periodic transfers.

Implication: Periodic transfers may be delayed or aborted. If the asynchronous retry latency causes the periodic transfer to be aborted, the impact varies depending on the nature of periodic transfer:

- If a periodic interrupt transfer is aborted, the data may be recovered by the next instance of the interrupt or the data could be dropped.
- If a periodic isochronous transfer is aborted, the data will be dropped. A single dropped periodic transaction should not be noticeable by end user.

Workaround: Intel recommends the use of the USB xHCI controller which is not affected by this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI26 USB EHCI FS/LS Incorrect Number of Retries

Problem: A USB low-speed transaction may be retried more than three times, and a USB full-speed transaction may be retried less than three times if all of the following conditions are met:

- A USB low-speed transaction with errors or the first retry of the transaction occurs near the end of a microframe, and there is not enough time to complete another retry of the low-speed transaction in the same microframe.
- There is pending USB full-speed traffic and there is enough time left in the microframe to complete one or more attempts of the full-speed transaction.
- Both the low-speed and full-speed transactions must be asynchronous (Bulk/Control) and must have the same direction either in or out.

Note: Per the USB EHCI Specification a transaction with errors should be attempted a maximum of three times if it continues to fail.

Implication: For low-speed transactions the extra retry(s) allow a transaction additional chance(s) to recover regardless of if the full-speed transaction has errors or not. If the full-speed transactions also have errors, the SoC may retry the transaction fewer times than required, stalling the device prematurely. Once stalled, the implication is software dependent, but the device may be reset by software.

Workaround: Intel recommends the use of the USB xHCI controller which is not affected by this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI27 USB EHCI RMH Think Time Issue

Problem: The USB RMH Think Time may exceed its declared value in the RMH hub descriptor register of 8 full-speed bit times.

Implication: If the USB driver fully subscribes a USB microframe, LS/FS transactions may exceed the microframe boundary.

Note: No functional failures have been observed.

Workaround: Intel recommends the use of the USB xHCI controller which is not affected by this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI28 USB EHCI Full-/low-speed Device Removal Issue

Problem: If two or more USB full-/low-speed devices are connected to the EHCI USB controller, the devices are not suspended, and one device is removed, one or more of the devices remaining in the system may be affected by the disconnect.

Implication: The implication is device dependent. A device may experience a delayed transaction, stall and be recovered via software, or stall and require a reset such as a hot plug to resume normal functionality.

Workaround: Intel recommends the use of the USB xHCI controller which is not affected by this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI29 Reported Memory Type May Not Be Used to Access the VMCS and Referenced Data Structures

Problem: Bits 53:50 of the IA32_VMX_BASIC MSR report the memory type that the processor uses to access the VMCS and data structures referenced by pointers in the VMCS. Due to this erratum, a VMX access to the VMCS or referenced data structures will instead use the memory type that the MTRRs (memory-type range registers) specify for the physical address of the access.

Implication: Bits 53:50 of the IA32_VMX_BASIC MSR report that the WB (write-back) memory type will be used but the processor may use a different memory type.

Workaround: Software should ensure that the VMCS and referenced data structures are located at physical addresses that are mapped to WB memory type by the MTRRs.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI30 A Page Fault May Not be Generated When the PS bit is set to "1" in a PML4E or PDPTE

Problem: On processors supporting Intel® 64 architecture the PS bit (Page Size bit 7) is reserved in PML4Es and PDPTEs. If the translation of the linear address of a memory access encounters a PML4E or a PDPTE with PS set to 1 a page fault should occur. Due to this erratum, PS of such an entry is ignored and no page fault will occur due to it is being set.

Implication: Software may not operate properly if it relies on the processor to deliver page faults when reserved Bits are set in paging-structure entries.

Workaround: Software should not set bit 7 in any PML4E or PDPTE that has Present bit (bit 0) set to "1".

Status: For the steppings affected, see the Summary Tables of Changes.

VLI31 CS Limit Violations May Not be detected after VM Entry

Problem: The processor may fail to detect a CS limit violation on fetching the first instruction after VM entry if the first byte of that instruction is outside the CS limit but the last byte of the instruction is inside the limit.

Implication: The processor may erroneously execute an instruction that should have caused a general protection exception.

Workaround: When a VMM emulates a branch instruction it should inject a general protection exception if the instruction's target EIP is beyond the CS limit.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI32 IA32_DEBUGCTL.FREEZE_PERFMON_ON_PMI is Incorrectly Cleared by SMI

Problem: FREEZE_PERFMON_ON_PMI (bit 12) in the IA32_DEBUGCTL MSR (1D9H) is erroneously cleared during delivery of an SMI (system-management interrupt).

Implication: As a result of this erratum the performance monitoring counters will continue to count after a PMI occurs in SMM (system-management mode).

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI33 PEBS Record EventingIP Field May be Incorrect after CS.Base Change

Problem: Due to this erratum a PEBS (Precise Event Base Sampling) record generated after an operation which changes CS.Base may contain an incorrect address in the EventingIP field.

Implication: Software attempting to identify the instruction which caused the PEBS event may identify the incorrect instruction when non-zero CS.Base is supported and CS.Base is changed. Intel has not observed this erratum to impact the operation of any commercially available system.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI34 Some Performance Counter Overflows May Not be logged in IA32_PERF_GLOBAL_STATUS When FREEZE_PERFMON_ON_PMI is enabled

Problem: When enabled, FREEZE_PERFMON_ON_PMI bit 12 in IA32_DEBUGCTL MSR (1D9H) freezes PMCs (performance monitoring counters) on a PMI (Performance Monitoring Interrupt) request by clearing the IA32_PERF_GLOBAL_CTRL MSR (38FH). Due to this erratum, when FREEZE_PERFMON_ON_PMI is enabled and two or more PMCs overflows within a small window of time and PMI is requested, then subsequent PMC overflows may not be logged in IA32_PERF_GLOBAL_STATUS MSR (38EH).

Implication: On a PMI, subsequent PMC overflows may not be logged in IA32_PERF_GLOBAL_STATUS MSR.

Workaround: Re-enabling the PMCs in IA32_PERF_GLOBAL_CTRL will log the overflows that were not previously logged in IA32_PERF_GLOBAL_STATUS.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI35 MOVNTDQA from WC Memory May Pass Earlier Locked Instructions

Problem: An execution of MOVNTDQA that loads from WC (write combining) memory may appear to pass an earlier locked instruction to a different cache line.

Implication: Software that expects a lock to fence subsequent MOVNTDQA instructions may not operate properly. If the software does not rely on locked instructions to fence the subsequent execution of MOVNTDQA then this erratum does not apply.

Workaround: Software that requires a locked instruction to fence subsequent executions of MOVNTDQA should insert an LFENCE instruction before the first execution of MOVNTDQA following the locked instruction. If there is already fencing or serializing instruction between the locked instruction and the MOVNTDQA, then an additional LFENCE is not necessary.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI36 Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results

Problem: The act of one processor or system bus master writing data into a currently executing code segment of a second processor with the intent of having the second processor execute that data as code is called cross-modifying code (XMC). XMC that does not force the second processor to execute a synchronizing instruction prior to execution of the new code is called unsynchronized XMC. Software using unsynchronized XMC to modify the instruction byte stream of a processor can see unexpected or unpredictable execution behavior from the processor that is executing the modified code.

Implication: In this case the phrase "unexpected or unpredictable execution behavior" encompasses the generation of most of the exceptions listed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide including a General Protection Fault (GPF) or other unexpected behaviors. In the event that unpredictable execution causes a GPF the application executing the unsynchronized XMC operation would be terminated by the operating system.

Workaround: In order to avoid this erratum programmers should use the XMC synchronization algorithm as detailed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide Section: Handling Self- and Cross-Modifying Code.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI37 SDIO Host Controller Does Not Control the SDIO Bus Power

Problem: The SD Bus Power bit in Power Control Register (Bus 0; Device 17; Function 0; Offset 029H) is not connected to any SOC IO pin that can reset the SDIO bus power. Due to this erratum, SDIO device Power-On-Reset cannot be controlled by Power Control Register. SDIO Controller may fail to comply with SD Host Controller Specification Version 3.00.

Implication: SDIO devices may not be powered up and initialized correctly.

Workaround: Software should be configured to use a GPIO pin on the platform to enable or disable the SDIO bus power. Refer to the Intel Atom® Processor E3800 Product Family SoC External Design Specification (EDS) document.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI38 USB HSIC Ports Incorrectly Reported as Removable

Problem: The DR (Device Removable) bit in the PORTSC registers of the two USB HSIC ports incorrectly indicates that devices on these ports may be removed.

Implication: Software that relies solely on the state of DR bits will consider fixed devices to be removable. This may lead the software to improper actions (e.g. requesting the user remove a fixed device).

Workaround: In conjunction with the DR bits, software should use BIOS-configured ACPI tables and factor in the CONNECTABLE field of the USB Port Capabilities object when determining whether a port is removable.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI39 Multiple Threads That Access the ISP Concurrently May Lead to a System Hang

Problem: The ISP (Image Signal Processor) may not be able to process concurrent accesses.

Implication: If multiple software threads access the ISP concurrently, it may lead to system hang during video recording, still image capture or preview modes.

Workaround: Avoid using multiple threads that may concurrently access the ISP. The Intel-provided drivers implement this workaround.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI40 Premature Asynchronous Interrupt Enabling May Lead to Loss of SDIO Wi-Fi Functionality

Problem: Setting the SDIO controller's Host Control 2 Register Asynchronous Interrupt Enable (Bus 0; Device 17; Function 0; Offset 03EH, bit 14) to '1' before the signal voltage switch sequence completion may result in SDIO card initialization failure.

Implication: SDIO card initialization failure may lead to software time out and loss of Wi-Fi device functionality. Currently released common operating system drivers do not use Asynchronous Interrupt mode.

Workaround: The SDIO driver should either use SDIO Synchronous Interrupt Mode or enable SDIO Asynchronous Interrupt Mode after the SDIO card signal voltage switch sequence completes.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI41 Paging Structure Entry May be Used Before Accessed And Dirty Flags Are Updated

Problem: If software modifies a paging structure entry while the processor is using the entry for linear address translation, the processor may erroneously use the old value of the entry to form a translation in a TLB (or an entry in a paging structure cache) and then update the entry's new value to set the accessed flag or dirty flag. This will occur only if both the old and new values of the entry result in valid translations.

Implication: Incorrect behavior may occur with algorithms that Atomically check that the accessed flag or the dirty flag of a paging structure entry is clear and modify other parts of that paging structure entry in a manner that results in a different valid translation.

Workaround: Affected algorithms must ensure that appropriate TLB invalidation is done before assuming that future accesses do not use translations based on the old value of the paging structure entry.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI42 Certain eMMC Host Controller Registers Are Not Cleared by Software Reset

Problem: Due to this erratum, when an eMMC Host Controller software reset is requested by setting bit 0 of the Software Reset Register (Offset 2FH), the Command Response Register (Offset 10H) and ADMA Error Status Register (Offset 54H) are not cleared. This does not comply with the SD Host Controller Specification 3.0.

Implication: Intel has not observed this erratum to impact any commercially available software.

Workaround: Software should not read these registers until a response is received from the eMMC device.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI43 LPE audio output not available on HDMI when HDAudio Controller is disabled

Problem: When LPE (Low Power Engine) audio is active, the HDAudio controller can be disabled. Due to this erratum, the LPE Audio is dependent on HDAudio controller being enabled.

Implication: HDMI will not output any audio when the HDAudio controller is disabled, and thus, will not play LPE audio where the LPE audio controller is selected by BIOS.

Workaround: The HDAudio controller should be enabled by soft-strap. BIOS should not disable it during the boot flow. Refer to the latest version of "Valleyview – I SoC BIOS Writers Guide".

Status: For the steppings affected, see the Summary Tables of Changes.

VLI44 USB Device Mode Controller May Not Successfully Switch to High-Speed Data Rate

Problem: The USB Device Mode Controller may initiate speed change to High-Speed data rate immediately following a reset of a discrete ULPI (UTMI+ Low Pin Interface) compliant PHY (physical layer) device.

Implication: Some ULPI-compliant PHYs may not recognize the USB Device Mode Controller speed change and thus may not be able to support USB High-Speed operation.

Workaround: None identified. Contact Intel technical support for information on supported PHY.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI45 USB Device Mode Controller Response Time May Exceed The Specification

Problem: The USB ULPI specification allocates 112-bit times for the USB Device Mode controller to respond to requests. Due to this erratum, the SoC's Device Mode controller may exceed this specification.

Implication: USB response time may exceed specifications in configurations with maximal total USB cable length, resulting in communication failure.

Workaround: Limit the total cable length used to connect to the host to less than 24m to compensate for the additional controller response time.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI46 USB Device Mode Controller May Not Enter the SS.Inactive State

Problem: When operating at SuperSpeed rates, the PENDING_HP_TIMER is used to detect lost or corrupted acknowledgments. The USB 3.0 specification requires a USB port to transition to the SS.Inactive state on the fourth consecutive timeout. Due to this erratum, the USB device mode controller in device mode will continue to enter Recovery state and not enter the SS.Inactive state.

Implication: This behavior does not comply with the USB 3.0 specification. Intel has not observed this erratum to impact the operation of any commercially available system.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI47 USB EHCI Full-/Low-speed Port Reset or Clear TT Buffer Request

Problem: One or more full-/low-speed USB devices on the same RMH controller may be affected if the devices are not suspended and either (a) software issues a Port Reset OR (b) software issues a Clear TT Buffer request to a port executing a split full-/low-speed Asynchronous Out command. The small window of exposure for full-speed device is around 1.5 microseconds and around 12 microseconds for a low-speed device.

Implication: The affected port may stall or receive stale data for a newly arrived split transfer occurring at the time of the Port Reset or Clear TT Buffer request.

Note: Note: This issue has only been observed in a synthetic test environment.

Workaround: Intel recommends the use of the USB xHCI controller which is not affected by this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI48 USB Device Mode Controller LFPS Transmission Period Does Not Meet USB 3.0 Specification

Problem: Upon USB Device Mode Controller SuperSpeed U1 (low-power state) exit, the LFPS (Low-Frequency Periodic Signaling) signal may be transmitted for less than the 600ns required by USB 3.0 specification.

Implication: In case of concurrent U1 exit by both sides of the USB link, there may be insufficient LFPS duration to ensure the exit is successful. In cases where U1 exit does not succeed, host software will typically initiate link recovery. Intel has not observed this erratum with any commercially available systems.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI49 Performance Monitor Instructions Retired Event May Not Count Consistently

Problem: Performance Monitor Instructions Retired (Event C0H; Umask 00H) and the instruction retired fixed counter (IA32_FIXED_CTR0 MSR (309H)) are used to track the number of instructions retired. Due to this erratum, certain situations may cause the counter(s) to increment when no instruction has retired or to not increment when specific instructions have retired.

Implication: A performance counter counting instructions retired may over or under count. The count may not be consistent between multiple executions of the same code.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI50 MTF VM Exit May be Delayed Following a VM Entry That Injects a Software Interrupt

Problem: If the "monitor trap flag" VM-execution control is 1 and VM entry is performing event injection, an MTF VM exit should be delivered immediately after the VM entry. Due to this erratum, delivery of the MTF VM exit may be delayed by one instruction if the event being injected is a software interrupt and if the guest state being loaded has RFLAGS.VM = CR4.VME = 1. In this case, the MTF VM exit is delivered following the first instruction of the software interrupt handler.

Implication: Software using the monitor trap flag to trace guest execution may fail to get a notifying VM exit after injecting a software interrupt. Intel has not observed this erratum with any commercially available system.

Workaround: None identified. An affected virtual machine monitor could emulate delivery of the software interrupt before VM entry.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI51 LBR Stack And Performance Counter Freeze on PMI May Not Function Correctly

Problem: When FREEZE_LBRS_ON_PMI flag (bit 11) in IA32_DEBUGCTL MSR (1D9H) is set, the LBR (Last Branch Record) stack is frozen on a hardware PMI (Performance Monitoring Interrupt) request. When FREEZE_PERFMON_ON_PMI flag (bit 12) in IA32_DEBUGCTL MSR is set, a PMI request clears each of the ENABLE fields of the IA32_PERF_GLOBAL_CTRL MSR (38FH) to disable counters. Due to this erratum, when FREEZE_LBRS_ON_PMI and/or FREEZE_PERFMON_ON_PMI is set in IA32_DEBUGCTL MSR and the local APIC is disabled or the PMI LVT is masked, the LBR Stack and/or Performance Counters Freeze on PMI may not function correctly.

Implication: Performance monitoring software may not function properly if the LBR Stack and Performance Counters Freeze on PMI do not operate as expected. Intel has not observed this erratum to impact any commercially available system.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI52 Certain MIPI CSI Sensors May Not Operate Correctly At Low Clock Frequencies

Problem: MIPI (Mobile Industry Processor Interface) CSI (Camera Serial Interface) DPHY may drop packets if the MIPI CSI clock frequency is below 80MHz and if camera sensor uses THS-Exit less than 200ns.

Implication: Intel has observed this erratum on systems using specific VGA sensors which operate at 80 MHz or lower and has THS-Exit less than 200ns.

Workaround: Do not operate sensor below 80MHz MIPI CSI clock with THS-Exit less than 200ns.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI53 USB Legacy Support SMI Not Available from xHCI Controller

Problem: SMIs are routed using the PMC (Power Management Controller) SMI_STS and SMI_EN registers. However, the USB SMI Enable (USB_SMI_EN) and USB Status (USB_STS) fields only reflect SMIs for the EHCI USB controller. SMIs triggered by the xHCI controller's USBLEGCTLSTS mechanism are not available.

Implication: BIOS is unable to receive SMI interrupts from the xHCI controller. BIOS mechanisms such as legacy keyboard emulation for pre-OS environments will be impacted.

Workaround: Use the EHCI controller for legacy keyboard emulation that requires legacy USB SMI support by BIOS.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI54 SD Card UHS-I Mode is Not Fully Supported

Problem: The SD Card Specification rev 3.01 Addendum 1 specifies a relaxed NCRC (Number of clocks to Cyclic Redundancy Check) timing specification for UHS-I (DDR50) mode. Due to this erratum, the SD Host Controller is not fully compatible with this relaxed timing specification.

Implication: Using UHS-I mode with SD devices that rely upon relaxed NCRC may cause SD host commands to fail to complete, resulting in device access failures.

Workaround: HS mode may be used in place of UHS-I. BIOS and driver workarounds have been identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI55 EOI Transactions May Not be Sent if Software Enters Core C6 During an Interrupt Service Routine - REMOVED

Status: Erratum has been fixed for all core processor steppings.

VLI56 USB xHCI May Execute a Stale Transfer Request Block (TRB)

Problem: When a USB 3.0 or USB 2.0 hub with numerous active Full-Speed (FS) or Low-Speed (LS) periodic endpoints attached is removed and then reconnected to a USB xHCI port, the xHCI controller may fail to fully refresh its cache of TRB records. The controller may read and execute a stale TRB and place a pointer to it in a Transfer Event TRB.

Implication: In some cases, the xHCI controller may read de-allocated memory pointed to by a TRB of a disabled slot. The xHCI controller may also place a pointer to that memory in the event ring, causing the xHCI driver to access that memory and process its contents, resulting in system hang, failure to enumerate devices, or other anomalous system behavior.

Note: This issue has only been observed in a stress test environment.

Workaround: None identified.

Note: A BIOS code change to reduce the occurrence of this erratum has been identified. Refer to the "Bay Trail – M/D SoC BIOS Writers Guide" or later.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI57 HD Audio Recording And Playback May Glitch or Stop

Problem: Under certain conditions generally involving extended simultaneous video and HD audio playback and/or recording, glitches, distortion, or persistent muting of the audio stream may occur due to improper processing of input stream data or response packets.

Implication: Due to this erratum, media device operation may not be reliable.

Workaround: A BIOS workaround has been identified to minimize the effect of this erratum. Please refer to the Bay Trail – M/D SoC BIOS Writers Guide or later. The third-party codec driver should minimize HD audio device command traffic.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI58 This erratum has been removed.

VLI59 SATA Signal Voltage Level Violation

Problem: SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the SATA transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specifications as defined in section 7.2.2.3 of the Serial ATA specification, rev 3.1. This issue applies to Gen 1 (1.5 Gb/s) and Gen 2 (3 Gb/s).

Implication: None known.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI60 PCIe Root Ports Unsupported Request Completion

Problem: The PCIe root ports may return an Unsupported Request (UR) completion with an incorrect lower address field in response to a memory read if any of the following occur:

1. Bus Master Enable is disabled in the PCIe Root Port's Command register (PCICMD bit 2 =0)
2. Address Type (AT) field of the Transaction Layer Packet (TLP) header is non-zero
3. The requested upstream address falls within the memory range claimed by the secondary side of the bridge
4. Requester ID with Bus Number of 0

Implication: The UR Completion with an incorrect lower address field may be handled as a Malformed TLP causing the Requestor to send an ERR_NONFATAL or ERR_FATAL message.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI61 VGA Max Luminance Voltage May Exceed VESA Limits

Problem: The max luminance voltage on the VGA video outputs may range from 640 mV to 810mV (the VESA specification range is 665 mV to 770mV) with linearity (INL/DNL) of up to ±3 LSB (the VESA linearity specification is ±1 LSB).

Implication: Intel has not observed any functional issues due to this erratum.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI62 SD Card Initialization Sequence May Fail When ACG is Enabled in SD Controller

Problem: When ACG (Auto Clock Gating) is enabled in SD controller, SDCLK may get turned off before voltage switch sequence is complete, possibly resulting in an initialization failure.

Implication: Intel has not observed this erratum to impact any commercially available software or system.

Workaround: A BIOS code change has been identified. Please refer to the latest version of “Intel Atom® processor E3800 product family Series based SoC, BIOS Writer's Guide”.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI63 Reset Sequence May Not Complete Under Certain Conditions

Problem: Under certain conditions, the SoC may not complete initialization either during a reset issued while the system is running or from the G3 (mechanically off) global system state.

Implication: When this erratum occurs, the SoC will detect an initialization problem and halt the initialization sequence prior to normal operation, leading to a system hang. The system will subsequently require a power cycle via the system power button.

Workaround: For the erratum occurring during reset while the system is running, a firmware code change has been identified which significantly reduces the likelihood of this erratum after the initial reset at power-on. For the erratum occurring while powering up from G3:

- For systems with EC (Embedded Controller) connected to PMIC, an EC Firmware workaround for the erratum is possible based on customer EC implementation.
- For systems without EC connected to PMIC, a hardware change may be implemented as a workaround for the erratum.

Contact your Intel representative on the guidance to implement these workarounds.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI64 Multiple Drivers That Access the GPIO Registers Concurrently May Result in Unpredictable System Behavior

Problem: The PCU (Platform Control Unit) in SoC may not be able to process concurrent accesses to the GPIO registers. Due to this erratum, read instructions may return 0xFFFFFFFF and write instructions may be dropped.

Implication: Multiple drivers concurrently accessing GPIO registers may result in unpredictable system behavior.

Workaround: GPIO drivers should not access GPIO registers concurrently. Each driver should acquire a global lock before accessing the GPIO register, and then release the lock after the access is completed. The Intel-provided drivers implement this workaround.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI65 Boot May Not Complete When SMI Occurs during Boot

Problem: During boot, the system should be able to handle SMIs (System Management Interrupt). Due to this erratum, boot may not complete when SMI occurs during boot.

Implication: If the system receives an SMI during boot, the boot may not complete.

Workaround: A BIOS workaround has been identified. Please refer to version 1.1 or later of "Intel Atom™ Processor E3800 Product Family SoC, BIOS Writer's Guide".

Status: For the steppings affected, see the Summary Tables of Changes.

VLI66 Interrupts That Target an APIC That is Being Disabled May Result in a System Hang

Problem: Interrupts that target a Logical Processor whose Local APIC is either in the process of being hardware disabled by clearing bit 11 in the IA32_APIC_BASE_MSR or software disabled by clearing bit 8 in the Spurious-Interrupt Vector Register at offset 0F0H from the APIC base are neither delivered nor discarded.

Implication: When this erratum occurs, the processor may hang.

Workaround: None identified. Software must follow the recommendation that all interrupt sources that target an APIC must be masked or changed to no longer target the APIC, and that any interrupts targeting the APIC be quashed, before the APIC is disabled.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI67 Corrected or Uncorrected L2 Cache Machine Check Errors May Log Incorrect Address in IA32_MCi_ADDR

Problem: For L2 Cache errors with IA32_MCi_STATUS.MCACOD (bits [15:0]) value 0000_0001_0000_1010b, the address reported in IA32_MCi_ADDR MSR may not be the address that caused the machine check.

Implication: Due to this erratum, the address reported in IA32_MCi_ADDR may be incorrect.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI68 Software-initiated Partition Reset May Cause a System Hang

Problem: When the software issues CF9H I/O port host partition reset, the SoC may hang during the reset sequence.

Implication: When this erratum occurs, the system may hang.

Workaround: A BIOS workaround has been identified which promotes the host partition reset to a Global Reset when the hang is detected. For the steppings affected, see the Summary Tables of Changes.

VLI69 Write-1-Clear Bits in PMC Registers May be Unexpectedly Cleared

Problem: Due to this erratum, writing certain PMC (Power Management Controller) registers with 8-bit, 16-bit, or non-naturally aligned 32-bit transfers may cause write-1-clear bits in adjacent fields to be unexpectedly cleared. The affected registers are: PRSTS, VLV_PM_STS, GEN_PMCON1, S0IX_WAKE_STS, PM1_STS_EN, GPE0a_STS, SMI_STS, ALT_GPIO_SMI, UPRWC, TCO_STS.

Implication: Write-1-clear bits are typically used to report interrupt-type events to software. Inadvertent clearing of these bits may prevent software from detecting events. Intel has not observed this erratum to impact the operation of any commercially available software.

Workaround: The affected registers should be written with naturally aligned 32-bit transfers. When the destination field is narrower than 32 bits, adjacent field(s) within the naturally aligned 32-bit boundary must also be written.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI70 Port Reset on USB2 Port0 And Port1 May Cause a Reset on HSIC Port0 and Port1 Respectively

Problem: HSIC Port0 - Port1 are dedicated to HSIC devices, while USB Port0 – Port3 can be used for USB devices. Due to this erratum, a traffic interrupt is caused on HSIC Port0 or HSIC Port1 when a Port Reset is issued by the driver on USB2 Host Port0 or USB2 Host Port1 respectively.

Implication: When this erratum occurs, the traffic interruption on HSIC Port0 or Port1 will result in a transaction error being reported by the HSIC host controller to the driver. The driver in response will re-enumerate the HSIC device causing it to reset.

Workaround: Configure USB and HSIC ports such that USB Port0 in USB2 host mode is not used simultaneously with HSIC Port0, and USB Port1 in USB2 host mode is not used simultaneously with HSIC Port1.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI71 Frequency Reported by CPUID Instruction May Not Match Published Frequency

Problem: When the CPUID instruction is executed with EAX = 80000002H, 80000003H, and 80000004H, the frequency reported in the brand string may be truncated while the published frequency is rounded. For example, a processor with a frequency of 1.4999GHz may be reported as 1.49GHz in the brand string instead of the published frequency of 1.5GHz.

Implication: Certain Intel Atom® Processor E3800 Product Family processors may report in brand string a frequency lower than the published frequency.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI72 Some USB Controller Capability Registers May Be Invalid After S3 Resume

Problem: The contents of several USB xHCI host capability registers may be invalid after an S3 Resume. Registers impacted by this erratum are HCCPARAMS, HCSPARAMS1, HCPARAMS3, USB2_PHY_PMC, USB_PGC, and XLTP_LTV1.

Implication: Software that depends on the contents of the named registers may not behave as expected, possibly leading to a USB driver failure or a system hang.

Workaround: A BIOS workaround has been identified. Please refer to the latest version of the BIOS spec update and memory reference code.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI73 Machine Check Status Overflow Bit May Not be Set

Problem: The OVER (error overflow) indication in bit [62] of the IA32_MC0_STATUS MSR (401H) may not be set if IA32_MC0_STATUS.MCACOD (bits [15:0]) held a value of 0x3 (External Error) when a second machine check occurred in the MC0 bank. Additionally, the OVER indication may not be set if the second machine check has an MCACOD value of 0x810, 0x820 or 0x410, regardless of the first error.

Implication: Software may not be notified that an overflow of MC0 bank occurred.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI74 Attempts to Clear Performance Counter Overflow Bits May Not Succeed

Problem: An MSR write which sets IA32_PERF_GLOBAL_OVF_CTRL MSR (390H) bits 1 and/or 0 may not clear the corresponding bit(s) of IA32_PERF_GLOBAL_STATUS MSR (38EH) if neither IA32_PMC0 nor IA32_PMC1 are enabled at the time of the MSR write and at least one of the fixed-function performance counters is enabled.

Implication: Software will not be able to rely on writes to this MSR to clear the overflow indication of the general-purpose performance counters.

Workaround: Software can avoid this erratum by disabling all fixed-function performance counters before writing to IA32_PERF_GLOBAL_OVF_CTRL MSR.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI75 SMI in 64-bit Mode May Store an Incorrect RIP to SMRAM When CS has a Non-Zero Base

Problem: On an SMI (system-management interrupt), the processor stores the RIP of the next instruction in SMRAM (system-management RAM). Due to this erratum, an SMI that occurs while the processor is in 64-bit mode with a non-zero value in the CS segment base may result in an incorrect RIP being stored in SMRAM.

Implication: When this erratum occurs, the RIP stored in SMRAM will be incorrect and the RSM instruction will resume from that incorrect RIP, resulting in unpredictable system behavior. Intel has not observed this erratum with any commercially available system.

Workaround: It is possible for the firmware to contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI76 VM Exit May Set IA32_EFER.NXE When IA32_MISC_ENABLE Bit 34 is Set to 1

Problem: When "XD Bit Disable" in the IA32_MISC_ENABLE MSR (1A0H) bit 34 is set to 1, it should not be possible to enable the "execute disable" feature by setting IA32_EFER.NXE. Due to this erratum, a VM exit that occurs with the 1-setting of the "load IA32_EFER" VM-exit control may set IA32_EFER.NXE even if IA32_MISC_ENABLE bit 34 is set to 1. This erratum can occur only if IA32_MISC_ENABLE bit 34 was set by guest software in VMX non-root operation.

Implication: Software in VMX root operation may execute with the "execute disable" feature enabled despite the fact that the feature should be disabled by the IA32_MISC_ENABLE MSR. Intel has not observed this erratum with any commercially available software.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI77 Top Swap Mechanism May Become Incorrectly Configured

Problem: Writing to the GCS (RCRB_GENERAL_CONTROL) register (RCRB_BAR, Offset 0x0) may cause the top swap mechanism to become incorrectly configured, resulting in unreliable boot behavior.

Implication: Due to this erratum, boot behavior may become unreliable which may impact system availability.

Workaround: It is possible for the firmware to contain a workaround for this erratum that disables the Top Swap mechanism.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI78 Certain Peripheral I/O Controllers May Hang After an Unexpectedly Long Latency Memory Transaction

Problem: When an eMMC (Embedded MultiMedia Card), LPE (Low Power Engine), xDCI (USB Device Mode Controller), SDIO (Secure Digital Input Output), or SD (Secure Digital) controller memory transaction encounters an unexpectedly long latency, this may cause the controller to hang.

Implication: When this erratum occurs, the peripheral I/O controller will hang.

Workaround: It is possible for the firmware to contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI79 Disabling SDIO or SDCARD May Lead To a System Hang

Problem: If BIOS disables either the SDIO or the SDCard (but not both) and follows the recommended sequence of placing the disabled controller in D3, the remaining enabled controller may stop functioning and hang the system. If BIOS doesn't put the disabled controller in D3, the enabled controller will operate normally but entry to the S0ix low-power state is blocked.

Implication: When this erratum occurs, the SDIO or the SDCARD stops functioning and may hang the system.

Workaround: It is possible for the firmware to contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI80 ULPI Bus Marginality for USB Device Mode

Problem: USB device mode is supported by the SoC via the ULPI (UTMI+ Low Pin Interface) bus. The ULPI bus may exhibit read timing marginalities resulting in a hold time violation.

Implication: Due to this erratum, the SoC ULPI reads may be unreliable.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI81 TLB Entries May Not Be Invalidated Properly When Bit 8 Is Set in EPT Paging-Structure Entries

Problem: EPT (extended page tables) translates guest-physical addresses to physical addresses using EPT paging structures. Bit 8 of each EPT paging-structure entry is available to software and should be ignored by the processor. Due to this erratum, the INVVPID and MOV to CR3 instructions may fail to invalidate TLB entries that were created using EPT paging-structure entries in which bit 8 was set.

Implication: The affected TLB entries may be incorrectly shared across linear-address spaces, possibly leading to unpredictable guest behavior.

Workaround: It is possible for the firmware to contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI82 CPUID Instruction Leaf 0AH May Return an Unexpected Value

Problem: When a CPUID instruction is executed with EAX = 0AH (Architectural Performance Monitoring Leaf), the value returned in EDX may incorrectly set bit 14. CPUID leaf 0AH EDX bit 14 is reserved and should be zero.

Implication: When this erratum occurs, the processor will report an incorrect value EDX.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI83 Video And/or Audio Artifact May Occur When Changing Frequencies

Problem: When changing the processor frequency, the SoC may fail to update the USB descriptor prior to xHCI consuming the descriptor when in ISOC mode.

Implication: When this erratum occurs, videos or audio artifacts may occur.

Workaround: It is possible for the firmware to contain processor configuration data and code changes as a workaround for this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI84 USB Device May Not be Detected at System Power-On

Problem: Certain internal conditions may cause the D-signal of one or more USB ports to get stuck at +3.3V during system power-on

Implication: When this erratum occurs, a USB device attached to the affected port will not function. In addition, the OS may report problems with the USB port. This erratum may not affect all SoCs and has been observed only on platforms that ramp the 1.8V sustain rail (V1P8A) before ramping the 3.3V sustain rail (V3P3A).

Workaround: A BIOS workaround has been identified. Refer to *USB 2.0 Device Lost During System Cold Boot - Technical Advisory*, Document# 556192.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI85 VM Exits During Execution of INTn in Virtual-8086 Mode with Virtual-Mode Extensions May Save RFLAGS Incorrectly

Problem: An APIC-access VM exit or a VM exit due to an EPT (Extended Page Table) violation or an EPT misconfiguration that occurs during execution of the INTn instruction in virtual-8086 mode (EFLAGS.VM = 1) with virtual-mode extensions (CR4.VME = 1) may save an incorrect value for RFLAGS in the guest-state area of the VMCS.

Implication: This erratum may cause a virtual machine monitor to handle the VM exit incorrectly, may cause a subsequent VM entry to fail, or may cause incorrect operation of guest software.

Workaround: It is possible for the firmware to contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI86 Clearing IA32_MC0_CTL[5] May Prevent Machine Check Notification

Problem: Clearing bit 5 of a logical processor's IA32_MC0_CTL MSR (400H) may incorrectly block notifying other logical processors of any local machine check.

Implication: The system may not react as expected to a machine check exception when IA32_MC0_CTL[5] is 0.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI87 System May Unexpectedly Reboot After Shutdown

Problem: Certain internal conditions may cause the system to reboot immediately after a shutdown.

Implication: A user shutdown request may not result in the system reaching a power-off condition.

Workaround: It is possible for the firmware to contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI88 Unusual waveform on SATA GEN1 (1.5 Gbps) during window loading

Problem: Abnormal idle waveform (666ps) observed intermittently during boot time (before window logon screen) on SATA_TX signal under gen 1 speed mode.

Implication: Intel has not observed this erratum to impact any SATA GEN1 functional features.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI89 System May Experience Inability to Boot or May Cease Operation

Problem: Under certain conditions where activity is high for several years the LPC, USB (low speed and full speed) and SD Card circuitry may stop functioning in the outer years of use.

Implication: LPC circuitry that stops functioning may cause operation to cease or inability to boot. SD Card or USB circuitry that stops functioning may cause SD Cards to be unrecognized or Low Speed or Full Speed USB devices to not function. Designs that implement the LPC interface at the 1.8V signal voltage are not affected by the LPC part of this erratum.

Workaround: Firmware code changes for LPC circuitry and mitigations for SD Card & USB circuitry have been identified and may be implemented for this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

VLI90 LPC Clock Control Using the ILB_LPC_CLKRUN# Signal May Not Behave As Expected

Problem: The ILB_LPC_CLKRUN# pin should be an input/open drain output signal as stated for the CLKRUN# signal in Section 2 of the Intel Low Pin Count (LPC) Interface Specification, Revision 1.1. Due to this erratum, if the signal is configured to be an output signal, the buffer may drive an active high level.

Implication: The processor may prevent a peripheral device from successfully requesting the LPC clock.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

VLI91 xHCI Host Controller Reset May Cause a System Hang

Problem: xHCI Host Controller may not respond following system software setting (Bit 1='1') the Host Controller Reset (HCRST) of the USB Command Register (xHCIBAR+80h).

Implication: CATERR# may occur resulting in a system hang.

Workaround: A 1 ms delay is necessary following system software setting (Bit 1='1') Host Controller Reset (HCRST) of the USB Command Register (xHCIBAR+80h).

Status: For the steppings affected, see the Summary Table of Changes.

VLI92 Shutdown May Occur When Memory Subsystem Signals a Machine Check Exception

Problem: A Machine Check Error signaled by the Memory Subsystem may cause the processor to enter shut down state instead of delivering a Machine Check Exception (#MC).

Implication: The processor may enter shut down state instead of delivering #MC, though the IA32_MCi_STATUS registers are correctly updated and persist through warm reset.

Workaround: It is possible for BIOS to contain a workaround for this issue

Status: For the steppings affected, see the Summary Table of Changes.

VLI93 LPE Audio Playback May Result in System Hang

Problem: Extended audio playback with the LPE (Low Power Engine) may result in a system hang if the SOC concurrently enters C6 or deeper sleep states.

Workaround: It is possible for the driver to contain a workaround for this erratum

Implication: The system may hang when this erratum occurs.

Status: For the stepping affected, see the Summary Tables of Changes.

VLI94 Transient SATA Gen 1 Signal Anomaly During OS Boot

Problem: When operating at SATA Gen 1 (1.5 Gbps), an anomalous SATA_TX electrical idle condition may occur for one unit interval (nominally 667ps) during operating system boot. This erratum does not affect operating at SATA Gen 2.

Implication: Intel has not observed this erratum to impact any commercially available system.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

VLI95 eMMC CRC Detection

Problem: The eMMC controller may fail to detect a CRC error if a bit error occurs on the DATA3 signal during read operations when in eMMC High-Speed DDR mode. CRC detection on other DATA signals is not impacted.

Implication: The controller will not flag the CRC error to the driver or application, which could result in data integrity issues. Bit errors on eMMC signals are not expected on platforms that follow Intel recommended design guidelines and tuning processes.

Workaround: None identified. To mitigate the issue, eMMC High-Speed SDR mode can be used instead of High-Speed DDR.

Status: For the steppings affected, see the Summary Table of Changes.

VLI96 xHCI Short Packet Event Using Non-Event Data TRB

Problem: The xHCI may generate an unexpected short packet event for the last transfer's Transfer Request Block (TRB) when using Non-Event Data TRB with multiples TRBs.

Implication: Transfer may fail due to the packet size error.

Note: This issue has only been observed in a synthetic environment. No known implication has been identified with commercial software.

Workaround: None Identified.

Intel recommends software to use Data Event TRBs for short packet completion.

Status: For the steppings affected, see the Summary Table of Changes.

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Specification Changes

1. Top Swap Feature

Due to Erratum VLI77 "Top Swap Mechanism May Become Incorrectly configured" the Top Swap capability is de-featured. Affected documents are:

Intel Atom® Processor E3800 Product Family Datasheet

2. TCO Timer Clock Period

The TCO timer period is incorrectly documented as approximately 0.6 seconds and should, instead, be approximately 1.0 seconds. The TCO_TMR.TCO_TRLD_VAL register field definition changes as follows:

TCO Timer reload value (TCO_TRLD_VAL) (tco_trld_val): Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0000h or 0001h will be ignored and should not be attempted. The timer is clocked at approximately 1 second, and thus allows timeouts ranging from 2 seconds to 1023 seconds.

Note: The timer has an error of +/- 1 tick (1.0s). The TCO Timer will only count down in the S0 state.

3. PCI Express Non-Common/Asynchronous Reference Clock Support

Support for non-common/asynchronous reference clocks on the processor root ports and the downstream device ports is de-featured. A downstream device must use the corresponding processor PCIE_CLKP/N clock pair as its reference clock. Affected documents are:

Intel Atom® Processor E3800 Product Family Datasheet

4. S4/S5 to S0 (Power Up) Sequence Specification Change

Note 5 from Table 61. S4/S5 to S0 (Power Up) Sequence of the *Intel Atom® Processor E3800 Product Family Datasheet*, Doc #538136, which specifies an alternate power-up sequence for the V1P0A & V1P8A rails, will be modified. The modified note will state:

Note: 5. An alternate SUS rail sequence allows swapping V1P8A with V1P0A. This sequencing should not be used for new designs.

5. Table 141. The setup of PCU_SPI_MISO with respect to serial clock falling edge at the host (t184) in PCU-SPI NOR AC Specification updates

Intel Atom® Processor E3800 Product Family Datasheet, Doc #538136, Section 9.6.20 PCU-SPI NOR AC Specification updates:

The setup of PCU_SPI_MISO with respect to serial clock falling edge at the host (t184) is changed from 11ns (min.) to 6ns (min.).

6. Table 171. Hardware Accelerated Video Decode Codec Support

Intel Atom® Processor E3800 Product Family Datasheet, Doc# 538136, Section 14.8.1 - Video Encode/Decode

Category	CODEC Format
Media decode rate	Up to 1080p@60 fps and 3x 4kx2k @ 30 fps (H.264/JPEG/MJPEG/MVC/MPEG-2/ WMV9/ VC1)
Media encode rate	Up to 1080p@60 fps

Specification Clarifications

1. GPU Frequency Encoding Description

The following clarification applies to the PUNIT_GPU_FREQ_STS.STATUSFREQID register field, which indicates the encoded frequency of the processor GPU. Table 1 defines the decoded frequency for possible encoded values.

Note: The decoded frequency varies depending on where the processor supports a DRAM transfer rate of 1333 MT/s or 1066 MT/s.

Table 3. GPU Frequency Encoding

Encoded Frequency	Decoded Frequency for Processor Supporting 1333 MT/s DRAM (MHz)	Decoded Frequency for Processor Supporting 1066 MT/s DRAM (MHz)
0xE7	1000	
0xE6	979	
0xE5	958	
0xE4	938	1000
0xE3	917	978
0xE2	896	956
0xE1	875	933
0xE0	854	911
0xDF	833	889
0xDE	813	867
0xDD	792	844
0xDC	771	822
0xDB	750	800
0xDA	729	778
0xD9	708	756
0xD8	688	733
0xD7	667	711
0xD6	646	689
0xD5	625	667
0xD4	604	644
0xD3	583	622
0xD2	563	600
0xD1	542	578
0xD0	521	556
0xCF	500	533
0xCE	479	511

Encoded Frequency	Decoded frequency for processor supporting 1333 MT/s DRAM (MHz)	Decoded frequency for processor supporting 1066 MT/s DRAM (MHz)
0xCD	458	489
0xCC	438	467
0xCB	417	444
0xCA	396	422
0xC9	375	400
0xC8	354	378
0xC7	333	356
0xC6	313	333
0xC5	292	322
0xC4	271	289
0xC3	250	267
0xC2	299	244
0xC1	208	222
0xC0	188	200
0xBF	167	178
0xBE		156

2. ECC Error Reporting Description

The Intel Atom® processor E3800 Product Family only supports memory ECC error reporting as an error count. No other form of error reporting is supported, including access to the error syndrome.

3. S4/S5 to S0 (Power Up) Sequence

Table 61. S4/S5 to S0 (Power Up) Sequence of the *Intel Atom® Processor E3800 Product Family Datasheet*, Doc #538136.

These timings are allowed to have an error of up to 5%. When no max timing is specified, the actual timing should be as close to the min timing as possible under normal operating conditions (typically within one additional unit of time), but no max timing is guaranteed.

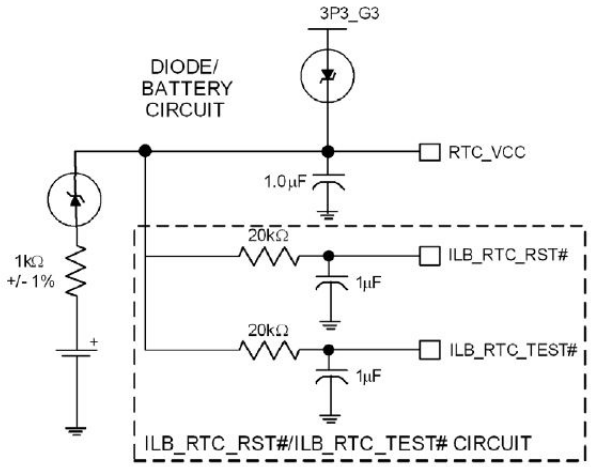
Documentation Changes

1. Statement of Volatility (SOV)

Intel Atom® Processor E3800 Product Family processors do not retain any end-user data when powered down and/or the processor is physically removed from the socket.

2. ILB_RTC_TEST# and ILB_RTC_RST# RC Time Delay Calculation Formula

The RC delay between RTC_VCC to ILB_RTC_TEST and ILB_RTC_RTC, Figure 21-4 in Section 21.2.3 of the PDG (Doc ID #512379) is obtained by using the formula t= - ln((RTC_VCC - Vih min)/RTC_VCC)*R*C and the added circuit is as follows:



The SoC RTC requires some additional external circuity. The ILB_RTC_RST# and ILB_RTC_TEST# signals are used to reset the RTC well. The external capacitor and the external resistor between ILB_RTC_RST#/ILB_RTC_TEST# and RTC battery (VBAT) were selected to create an RC time delay, such that ILB_RTC_RST# and ILB_RTC_TEST# go high sometime after the battery voltage is valid. The RC time delay should be in the range of 18-25 ms. When ILB_RTC_TEST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_1 (General PM Configuration 1) register is set to 1, and remains set until software clears it. Hence, when the system boots, the BIOS recognizes that the RTC battery is removed.

3. eMMC* 5.0 Functional Backward Compatibility Support Notes

A note will be added in Section 14 *Intel Atom® Processor E3800Product Family - Platform Design Guide*, Doc ID 512379 as follows:

14 Embedded MultiMedia Card (eMMC*)

The eMMC* controller supports mass storage devices with a stack of software that manages the physical connection of the device to the bus and the translation of the commands from the system to the device. It conforms to the eMMC* v4.41 and v4.51 standard.

Note: eMMC 5.0 is functionally backward-compatible on the Bay Trail platform as per eMMC 4.5, without the guarantee that performance is as good as eMMC 4.5.

4. Remove PCU- SPI AC Specification Section

Intel Atom® Processor E3800 Product Family Datasheet, Doc #538136, Section 9.6.19 PCU-SPI AC Specification updates:

Section 9.6.19 PCU-SPI AC Specification is to be removed as the Intel Atom® Processor E3800 Product Family does not support serial clock frequency of 25 MHz. The removal includes Table 140 PCU-SPI AC Specification and Figure 67 SPI AC Timing.

Refer to Section 9.6.20 PCU-SPI NOR AC Specification is valid and should be used for reference.

5. Start Address and End Address Corrections for High Precision Event Timer (HPET)

Intel Atom® Processor E3800 Product Family Datasheet, Doc #538136, Section 4.1.2 IO Fabric (MMIO) Map.

The Start Address and End Address for HPET should be revised as below:

Table 42. Fixed Memory Ranges in the Platform Controller Unit (PCU)

Device	Start Address	End Address	Comments
Low BIOS (Flash Boot)	000E0000h	000FFFFFh	Starts 128 KB below 1 MB; Firmware/BIOS
IO APIC	FEC00000h	FEC00040h	Starts 20 MB below 4 GB
HPET	FED00000h	FED003FFh	Starts 19 MB below 4 GB
TPM (LPC)	FFD40000h	FFD40FFFh	Starts 16 KB above HPET range
High BIOS/Boot Vector	FFFF0000h	FFFFFFFFh	Starts 64 KB below 4 GB; Firmware/BIOS

6. CPU Base Clock (BCLK) Frequency

The CPU frequency of each processor core is a multiplication of the CPU Base Clock (BCLK) frequency. The following table shows the BCLK frequency for each SKU;

Table 1. BCLK Frequencies

Processor SKU	Base Clock (BCLK) Frequency (MHz)
E3845	$83.\dot{3}$
E3827	$83.\dot{3}$
E3826	$133.\dot{3}$
E3825	$133.\dot{3}$
E3815	$133.\dot{3}$
E3805	$133.\dot{3}$

Note: The dot on top of the number is to show that it’s recurring.

7. 1.4.2 Intel Atom® Processor E3800 Product Family - Datasheet, Document# 538136, Section 9.6.22 PCU -iLB - LPC AC specification, Table 144 correction.

Numbering for corresponding figures mentioned are wrong and should be corrected as below;

Table 144. LPC AC Specifications (with loop back ILB_LPC_CLK[0] to ILB_LPC_CLK[1])

Sym	Parameter	Min	Max	Units	Notes	Fig
TCO	ILB_LPC_AD[3:0], ILB_LPC_FRAME#, ILB_LPC_SERIRQ Valid Delay from ILB_LPC_CLK[1] Rising	2	14	ns		71
T EN_AD	ILB_LPC_AD[3:0], ILB_LPC_FRAME#, ILB_LPC_SERIRQ Output Enable Delay from, ILB_LPC_CLK[1] Rising	2		ns		72
T FD_AD	ILB_LPC_AD[3:0], Float Delay from, ILB_LPC_CLK[1] Rising		28	ns		73
T SU_AD	ILB_LPC_AD[3:0], Setup Time to ILB_LPC_CLK[1] Rising	7		ns		74
T HD_AD	ILB_LPC_AD[3:0], Hold Time from, ILB_LPC_CLK[1] Rising	0		ns		74
T lpc	ILB_LPC_CLK[1:0] Duty Cycle	35	65	%	1	

8. Thermal Sensor

Intel Atom® Processor E3800 Product Family Datasheet, Doc #538136, Section 8.2 Thermal Sensors will be updated as follows:

Note: DTS accuracy is ± 8°C for < 60°C and is ± 6°C for > 60°C

9. 7.2.1 RTC Power Well Transition (G5 to G3 States Transition)

Intel Atom® Processor E3800 Product Family Datasheet, Doc #538136, Section 7.2.1 RTC Power Well Transition (G5 to G3 States Transition) updates:

RTC_VCC to ILB_RTC_TEST# and ILB_RTC_RTC# de-assertion (t1) min value is changed from 18ms to 9ms.

Table 60. RTC Power Well Timing Parameters

Parameter	Description	Min	Max	Unit
t1	RTC_VCC to ILB_RTC_TEST# and ILB_RTC_RTC# de-assertion	9	-	ms

10. 7.2.2 G3 to S0

Intel Atom® Processor E3800 Product Family Datasheet, Doc #538136, Section 7.2.2 G3 to S0 updates:

Add superscript number 14, 15, 16 to RTC_VCC to ILB_RTC_TEST# and ILB_RTC_RST# deassertion RTC_VCC to PMC_RSMRST# de-assertion (t1) min value.

Table 61. S4/S5 to S0 (Power Up) Sequence

Parameter	Description	Min	Max	Unit
t1	RTC_VCC to ILB_RTC_TEST# and ILB_RTC_RST# deassertion RTC_VCC to PMC_RSMRST# de-assertion	9[14,15,16]	-	ms
t2	V3P3A (SUS Rails) valid to PMC_RSMRST# de-assertion (t1 still applies in applications without RTC battery)	10	-	us
t3	PMC_RSMRST# to Internal RTC Clock assumed stable	95		ms
t4	Internal RTC Clock assumed stable to PMC_SUSCLK[0] toggling	5		ms
t5	PMC_SLP_S4# de-assertion to PMC_SLP_S3# deassertion	30	-	us
t6a	Core well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion (No PCIe devices)	10	-	ms
t6b	Core well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion (for power rails needed by PCIe devices)	99	-	ms
t7	DRAM/PMC_CORE_PWROK to PMC_SUS_STAT#	1	-	ms
t8	PMS_SUS_STAT# de-assertion to PMC_PLTRST# deassertion	60	-	us
tx	PMC_SLP_S4# de-assertion to VDDQ ramp start	0	-	ms

Notes:

14. RTC_VCC = 2.0V to the point in time where voltage on the RTC resets equals 0.65 times the voltage present on the RTC_VCC rail during ramp. This measurement should be made from RTC_VCC = 2.0V to the first of ILB_RTC_TEST# or ILB_RTC_RST# reaching 0.65 * RTC_VCC.

15. C3 and C4 Capacitors used in the RTC external circuit should be evaluated with regards to aging, voltage and temperature characteristics to ensure reliable operation in the intended operating environment. See section 38.2.3 External Capacitors.

16. For measurement details, please contact your Intel representative.

11. 9.5.14 PCU – iLB – LPC DC Specification

Intel Atom® Processor E3800 Product Family Datasheet, Doc #538136, Section 9.5.14 PCU – iLB – LPC DC Specification updates:

Add missing ILB_LPC_CLK [1:0] to the title in Table 94 and Table 95

Table 94. LPC Signal Group DC Specification (LPC_V1P8V3P3_S = 1.8V (ILB_LPC_AD][3:0], ILB_LPC_FRAME#, ILB_LPC_SERIRQ, ILB_LPC_CLKRUN#, ILB_LPC_CLK[1:0]))

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IH}	Input High Voltage	1.27	1.8	1.8 + 0.1	V	
V_{IL}	Input Low Voltage	-0.1	0	0.58	V	
V_{OH}	Output High Voltage	0.9 X 1.8			V	
V_{OL}	Output Low Voltage			0.1 X 1.8	V	
I_{OH}	Output High Current		1.5		mA	
I_{OL}	Input Low Current		-0.5		mA	
I_{LEAK}	Input Leakage Current			30	µA	
C_{IN}	Input Capacitance	1		9	pF	

Table 95. LPC Signal Group DC Specification LPC_V1P8V3P3_S = 3.3V (ILB_LPC_AD[3:0], ILB_LPC_FRAME#, ILB_LPC_CLKRUN#, ILB_LPC_CLK[1:0])

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IH}	Input High Voltage	0.5 X 3.3 + 0.7	3.3	3.3 + 0.1	V	1
V_{IL}	Input Low Voltage	-0.1	0	0.5 X 3.3 - 0.7	V	2
V_{OH}	Output High Voltage	0.9 X 3.3			V	3
V_{OL}	Output Low Voltage			0.1 X 3.3	V	3
I_{OH}	Output High Current		1.5		mA	3
I_{OL}	Input Low Current		-0.5		mA	3
I_{LEAK}	Input Leakage Current			30	µA	
C_{IN}	Input Capacitance	1		9	pF	

Notes:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value, Applies to ILB_LPC_AD[3:0], ILB_LPC_CLKRUN#
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value. Applies to ILB_LPC_AD[3:0], ILB_LPC_CLKRUN#
3. V_{OH} is tested with Iout=500uA, VOL is tested with Iout=1500uA
4. Applies to ILB_LPC_AD[3:0],ILB_LPC_CLKRUN# and ILB_LPC_FRAME#
5. ILB_LPC_SERIRQ is always a 1.8V I/O irrespective of the value of LPC_V1P8V3P3_S.

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